Broadband Amplifier Design

Design const. gain amp over a broad frequency range; usually a matter of properly designing the matching networks or feedback network to compensate for variation of $|S_{21}|$ with frequency.

Synthesis procedure can become quite involved.

Difficulties:

1. $|S_{21}|$ and $|S_{12}|$ vary with frequency (sketch)
2. S_{11}, S_{22} also vary with freq.
3. noise figure F and SWR will degrade in some region of freq. in a broadband amp.

Techniques: a) compensated MN, b) negative feedback.

So far design considered: stability, gain, noise figure, SWR. Now we consider their freq. variation. We need computer help very quickly! Some initial design done by hand and then switch to CAD.

Design procedure by Mellor involves the use of an interstage matching network. Fig. 4.4.1.

I/O matching networks designed with const. gain over the bandwidth. The interstage part provides "gain" that increases over the BW to compensate for $|S_{21}|$ decrease. $\Rightarrow$ flat gain.

Example of simple broadband design: ex. 4.4.1. S-matrix given, design amp with $G_T = 10$ dB over 300– 00 MHz. What about S_{12}? Assumed $=0$.

- find the "intrinsic gain" of BJT: $|S_{21}|^2 = 13$ dB (300 MHz), 10 dB (450), 6 dB (00). To flatten the gain: matching networks should have 3 dB decrease at 300 MHz, 0 dB at 450 MHz and 4 dB gain at 00 MHz.

  Since transistor is unilateral $\Rightarrow$ independent optimization of input and output matching

- what is the most gain we can get from I/OMN? Calculate

$$G_{s,max} = \frac{1}{1 - |S_{11}|^2} \quad G_{L,max} = \frac{1}{1 - |S_{11}|^2} \tag{1}$$

  For $G_{s,max} = 0.4, 0.3, 0.1$ dB $\Rightarrow$ not worth matching the input!

- on output: $S_{22} \approx 0.85$ over the BW. $\Rightarrow G_{L,max} = 5.6$ dB which makes 4 dB at 00 MHz possible.

- construct const. gain circles for -3 dB, 0 and 4 dB at 300, 450 and 00 MHz. (remember the procedure? is this uncond. stable?

  recall:

  – find S_{22}^* and draw line from origin to it. At S_{22}^* we have $G_L = G_{L,max}$

  – find G_L-s and g_L-s

  – calculate d_L, R_L

0 dB circle goes through origin. Matching network should transform 50 Ohm load into s[illegible]

- choose pts that can be generated by some simple circuit, e.g. ell circuit. One choice is hunt and series inductor added to 50 Ohm load.
- shunt inductor moves admittance along the const. conductance circle (shown in S-chart) but we have three different pts for three frequencies. Series L then moves impedance to the pts on G_L circles.
- How to pick up pts A, B, C? Trial and error until at least two freq. (say, lowest and highest) work out. For L_1 at 300 MHz we have $50/\ \omega L_1 = -\ 1.2 \Rightarrow L_1 = 22.1nH$.

  For L_2 use the highest freq.: $\omega L_2/50 = \ (3.2 - 0.4) \Rightarrow L_2 = 31.8$ nH. See fig. 4.4.3.

- on input: 50 Ohm source directly to input of BJT $\Rightarrow G_s =$ dB? $SWR = (1 + |S_{11}|)/(1 - |S_{11}|) = 1.86$ which could be improved but it has little influence on G_s.
- No guarantee that SWR (mismatch) is going to be small. What's to be done?

Balanced amps

Practical method to obtain broadband amp with flat gain and good I/O SWR. Figs. 4.4.5. Various 3-dB couplers: 3-dB Lange coupler fig. 4.4.6 and 3-dB branch-line coupler. For Lange: psecify freq., susbtrate, spacing d and w. Outputs at 2 and 3 are 90° out of phase.

50 Ohm source + 50 Ohm loads $\Rightarrow$ incident wave on 1 appears as $a_1/\sqrt{2}\exp(-\ \pi/2)$ on 2 and on 3 it has π phase. Power on input port is equally divided between ports 2 and 3 and nothing goes to port 4. The input is matched when all the other ports are 50 Ohms.

Reverse the operation: put two signals with $\pi/2$ difference on 2 and 3 $\Rightarrow$ summ appears on 1, i.e. 2x power.

Reflected part of the wave on input is coupled to port 4 but not to 2. $\Rightarrow$ reflected signals (due to mismatch) on I/O are directed into 50 Ohm loads.

For $\lambda/4$, 3-dB Lange coupler:

$$|S_{11}| = \frac{1}{2}|S_{11a} - S_{11b}|, \quad |S_{12}| = \frac{1}{2}|S_{12a} + S_{12b}| \tag{2}$$

$$|S_{21}| = \frac{1}{2}|S_{21a} + S_{21b}|, \quad |S_{22}| = \frac{1}{2}|S_{22a} - S_{22b}| \tag{3}$$

For identical amps $\Rightarrow S_{11} = S_{22} = 0$. Also, S_{21}, S_{12} are equal to one side of the coupler.

BW limited by the coupler — about 2 octaves.

Advantages:

- No worry about individual amp's SWR; concentrate instead on flat gain, F, gain etc. I/O SWR will be ≈ 1 (ideal case)
- high degree of stability
- output power 2x that of one amp
- even if one amp fails, balanced amp will still operate but with reduced gain
- ease of cascading — each unit is isolated!

Disadvantages: a) two amps needed, b) dc power consumption, c) bulk. Ex. 4.4.1.

Wilkinson 3-dB coupler, fig. 4.4.8. Divides equally input power on 1 between 2 and 3, when ports match terminated. Signals on 2 and 3 are of equal magnitude and phase.

Idea: For 2 and 3 terminated in 50 Ohms, 1 should see 50 Ohms $\Rightarrow$ each $\lambda/4$ line should transform 50 to 100 Ohm (why?). Use 0. Ohms line for this purpose. If equal loads are on 2 and 3, nothing goes through 100 Ohm resistor. When mismatch is present, cancellation occurs at the other output port. Also used as power combiner.

Negative feedback

Provides flat gain and reduces I/O SWR; also controls variations due to transistors. It has wide BW ($>$ 2 decades) but degrades noise figure F and G-s.

Fig. 4.4. , 8 and 9. What are the new S-parameters for the circuit?

$$S_{11} = S_{22} = \frac{1}{D}\left[1 - \frac{g_m Z_0^2}{R_2(1+g_m R_1)}\right] \tag{4}$$

$$S_{21} = \frac{1}{D}\left[\frac{-2g_m Z_0}{1+g_m R_1} + \frac{2Z_0}{R_2}\right] \tag{5}$$

$$S_{12} = \frac{2Z_0}{DR_2}, \quad D = 1 + \frac{2Z_0}{R_2} + \frac{g_m Z_0}{R_2(1+g_m R_1)} \tag{6}$$

For I/O SWR=1 we need $S_{11} = S_{22} = 0 \Rightarrow 1+g_m R_1 = f_m Z_0^2/R_2$ $\Rightarrow R_1 = Z_0^2/R_2 - 1/g_m$.

This produces $S_{21} = (Z_0 - R_2)/Z_0$ and $S_{12} = Z_0/(R_2 + Z_0)$.

An interval for R_1, R_2 can be determined that will give $S_{11} = S_{22} = 0$ with positive values. Take example of $|S_{21}|^2 =$ 10 dB in 50 Ohm system

$$g_{m,min}(R_1 = 0) = \frac{1 - S_{21}}{Z_0} = \frac{1 - (-3.16)}{50} = 83mS \qquad (7)$$

(- sign for $180°$ phase). Then for $R_1 = 0 \Rightarrow R_2 = g_m Z_0^2 = 208$Ohms.

If both resistors are used, then minimum I/O SWR is for $R_1 R_2 \approx Z_0^2$ but we need high g_m for that work out!

What about phase of S_{21}? For negative feedback it should be $\approx 180^\circ$ or at least it should not be less than 90° (otherwise?).

Most transistors have $\angle S_{21}$ that is 180° and stays const. but then falls off toward or through 90°.

Need some compensation to increase the phase; say, series L with R_2 reduces feedback at higher frequencies.

Eventually, we need CAD tools.

Example 4.4.2 (figs. 4.4.11 and 12). Gain is required to be $G_T = 10$ dB from 10 to 1500 MHz.

- lots of power available, certainly at LF but it is potentially unstable ($k < 1$)
- for $f > 1250$ MHz $\Rightarrow \angle S_{21} < 90^\circ$
- look at the frequency stability table
- 300 Ohm in shunt on output provides unconditional stability (except at 250 MHz). Power gain reduced, but still OK
- S_{11}, S_{22} still large $\Rightarrow$ I/O SWR poor; also, $\angle S_{21} < 90^\circ$ above 1250 MHz.

- Using $R_1 = 0 \Rightarrow R_2 = Z_0(1 + |S_{21}|) = 208$ Ohms.
- fix the phase of S_{21} by adding L in series with R_2. Take the corner frequency to be 1250 MHz, i.e. $R_2 = \omega L \Rightarrow L_2 = 28nH$. Figs. 4.4.13 and 14.
- match really attained only at one frequency and mismatch elsewhere.

Fano derived a set of integrals that predict the gain-BW restrictions for a set of lossless matching networks, which can be used to optimize the matching across the BW.

High Power Amplifier Design

So far: everything based on **small signal S-parameters**. Not very useful for high power design due to non-linearities. OK for class A, but not for AB, B or C.

Problem: large signal S-parameters not well defined and not easy to measure. Characterization done by source and load reflection coeff. as a function of output power and gain.

Special case: measurement of Γ_s and Γ_L together with output power when transistor is operated at its 1-dB compression point.

Definition of 1-dB compression point ($\Gamma 1db$): Power gain where the nonlinearities of the transistor reduce its power gain by 1 dB over the small signal power gain: $\Gamma 1db = G_0(\text{dB}) - 1$.

$$G_p = \frac{P_{out}}{P_{in}} \Rightarrow P_{out}(\text{dBm}) = G_p(\text{dB}) + P_{in}(\text{dBm}) \tag{8}$$

so that when output power is at 1 dB compression point:

$$P_{out}(\text{1dB}) = \Gamma 1db(\text{dB}) + P_{in}(\text{dBm}) = G_0(\text{dB}) - 1 + P_{in}(\text{dBm}) \tag{9}$$

$$\Rightarrow P_{\text{1dB}}(\text{dBm}) - P_{in}(\text{dBm}) = G_0(\text{dB}) - 1 \tag{10}$$

i.e. 1 dB comp. pt. is that point at which the output power minus the input power (in dBm) is equal to the small signal power gain minus 1 dB. (sketch)

$P_{o,mds}$ = minimum detectable signal power (noise limited). Input signal ($P_{i,mds}$)detectable only if its output power level ($P_{o,mds}$) is above noise power level.

Recal the thermal noise power of two port with noise figure F:

$$F = \frac{P_{No}}{P_{Ni}G_A}, \; P_{Ni} = kTB, \Rightarrow P_{No} = kTBG_AF \tag{11}$$

$kT = -174$dBm ; min. detectable signal on input is some number (X= typically 3) dB-s above thermal noise, then

$$P_{i,mds} = -174(\text{dBm}) + 10logB + F(\text{dB}) + X(\text{dB}) \tag{12}$$

$$P_{o,mds} = P_{i,mds} + G_A\text{dB}) \tag{13}$$

Dynamic range = where amplifier has linear power gain.