The Design and Layout of a Direct Broadcast Satellite (DBS)

Intermediate Frequency Amplifier

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ABSTRACT

TriQuint Semiconductor's (TQS) Gallium-Arsenide (GaAs) HA2 process was the basis for the design, simulation and manual layout of a 0.950 GHz to 1.450 GHz Class A intermediate frequency (IF) amplifier. A common source/common gate (cascode) gain stage wherein the currents of the two devices were independently set was chosen for the design. Two of these stages along with interstage and output buffering (current source biased source followers) were cascaded to form the IF amp. Extensive simulation was performed using MicroSim's 7.1 Release Pspice evaluation version software running on a Pentium-Pro processor. In order to meet the gain ripple specification of +\- 0.5 dB, shunt/shunt negative feedback was applied around the first cascode/buffer stage. The following table summarizes the performance of this IF amp.

DBS IF Amp Performance

Item	Value
supply	single: 15V
power gain	47.3+/-0.3 dB
peak V_o	1.2 V_{pp}*
power into 75 ohms	10 mW*
$\|Z_{IN}\|$	55 ohms*
$\|Z_o\|$	200 ohms*
$gamma_{out}$	0.53*
P_{DISS}	1.7 W

* At band center of 1.2 GHz.

A manual layout of the IF amp was performed using TQS's HA2 layout subcircuit library (tqha2fv2.sf) in Hewlett-Packard's Microwave Design System (MDS) simulation environment. The following table lists the layout subcircuits manually created using TQS's device layouts as a guide for the IF amp.

Manually Created Layout Subcircuits

Subcircuit/Device	Derivation
fet300: 300 um wide dFET* (6X50 um)	TQS's pbf510 and pdhss50 symmetric dFET "fingers"
fet200: 200 um wide dFET (4X50 um)	pared down version of fet300
fet20: 20 um wide dFET	"stretched" TQS pdhss50
rn10000, rn4000, rn3500 rn500: thinfilm nichrome resistors	stretched TQS rn10
cap10: 10 pF MIM capacitor (130 um X 130 um)	stretched TQS pcap50
diode150: 150 um wide N+ overlap diode	stretched TQS ps15p15
pad100: 100 um X 100 um bond pad	unaltered TQS ppad100

*All dFETs are depletion mode GaAsFETs with 0.5 um gate lengths.

The layout was converted to a GDSII file and submitted to TQS for a design rule check (DRC). The layout passed DRC with only minor revision.

Finally, bondwire inductance (~0.5 nH) was included in the design verification/simulation. Even the smallest amount of supply/ground line inductance had a profound effect on the frequency response and output reflection coefficient. Consequently, five pads were dedicated to V_{DD} and seven to ground for this layout.

DESIGN

Note: All figures referred to are found in the FIGURES section of this report.

A. GaAs Field Effect Transistor (GaAsFET) Characterization.

The quiescent drain current can be modeled as

$$I_D \sim BW(V_{GS} - V_T)^2$$

where the threshold or turn-on voltage goes as $V_T = V_{TO} - \text{gamma}*V_{DS}$. The symbols are defined as

B = transconductance parameter
W = width of the GaAsFET (usually in microns)
V_{GS} = gate to source potential
V_{TO} = intrinsic threshold voltage
gamma = threshold shifting parameter
V_{DS} = drain to source potential .

It turns out that linearization of the FET model (for AC calculation) produces a FET model that has a voltage dependent current source that has a gain of

$$g_m \sim 2BW(V_{GS} - V_T)$$

in parallel with a resistance

$$r_{ds} \sim 1/\text{gamma}*g_m \quad \text{(dynamic drain resistance).}$$

The dynamic drain resistance of these short channel devices is quite low compared with the corresponding quantity in bipolar devices (~ 300 ohms) but the typical g_m is high (~ 35 mS at I_D's of tens of milliamps) as compared with metal oxide semiconductor (MOS) FETs and junction FETs.

From these formulae it can be seen that, in general, there is a trade-off between g_m and r_{ds}. Since g_m is proportional to I_D, a high current source gain (g_m) leads to a lower r_{ds} which lowers the voltage available across the current source (in the linearized model).

B. A Two Stage Buffered Common Source (CS) Amplifier.

The voltage gain, $A_v=v_o/v_i$, derived from a simplified, low frequency linear model of a CS FET amplifier (stage) can be shown to be

$$A_v = -g_m*r_d$$

where g_m is, in addition to the above description, the slope of the I_D versus V_{GS} curve of the given FET at the operating point and r_d is the equivalent resistance the drain sees to ground under AC conditions. High I_{DQ} ensures higher g_m for a given device, thus, one would operate the GaAsFET at near maximum I_D (i.e., near I_{DSS} which occurs for V_{GS}=0V) to maximize the gain. It is also obvious that maximizing r_d will ensure a maximized gain. It should be noted that r_d is typically composed of a parallel combination of r_{ds}, the drain bias resistor, R_D, and the input impedance of the next stage. Unfortunately a high I_D leads to a lowered r_{ds} and excessive drops across R_D.

The two stage buffered CS amplifier of Figure 1 was designed and simulated to determine if it could produce a power gain of sufficient magnitude. It can be shown that the power gain of an amplifier is related to its voltage gain as

$$P_{dB} = 20\log(A_v) + 10\log(R_{IN}/R_L) = A_{vdB} + 10\log(R_{IN}/R_L) \quad .$$

Letting v_i = 1V and noting that $R_{IN} \sim R_L$=75 ohms gives $P_{dB} \sim v_{odB}$. Thus, a simulation output of v_{odB} gives a very close approximation of P_{odB} in this case.

A simulation of the buffered two stage CS amp of Figure 1 was performed using MicroSim's Pspice 7.1 evaluation package (it allows only single page schematics of up to 64 nodes). The TQS HA2 device library was loaded from which the HHSSgd GaAsFET model came. The circuit produced a driver I_D of ~ 22 mA and a buffer I_D of ~ 32 mA using the device widths of 300 um and 200 um respectively (I_D is proportional to W as shown above). Figure 3 shows the power gain performance of this amplifier. As can be seen, its low value of ~ 17 dB into 75 ohms and large variation over the IF band makes it unsuitable for this application. Adding more stages is possible but this, of course, adds to circuit complexity, power dissipation and device count.

C. Cascode Two Stage Amplifier.

The amplifier of Figure 2 was simulated in the same environment. A simple AC model is shown in Figure 4 for a single cascode stage.

The source diodes (Figure 2) attached to the 300 um devices set V_{GS} which, in turn, sets I_D to first order. The drop across R_2 and the five-diode string determine V_{GS} for the 20 um FETs. Thus, one must simultaneously choose $V_{GS,300}$, R_2 and $V_{GS,20}$ such that a reasonable $V_{DS,300}$ occurs (i.e., saturation operation) and that most of $I_{D,300}$ is supplied by $R_2(R_{13})$ keeping $I_{D,20}$ rather low. This is because the fet300's output sees approximately

$$r_{ds1} \,||\, R_2 \,||\, Z_{IN,CG}$$

where $Z_{IN,CG}$ is the impedance looking in the input (i.e., source) of the common gate (CG) stage. It can be shown that $Z_{IN,CG} \sim 1/g_m$, thus, one requires I_D to be small in order to not excessively load the CS drain. However, CG voltage gain is proportional to g_m (not $1/g_m$) which forces a compromise for the value of $g_{m,20}$. All the while the low GaAsFET r_{ds} (~ $1/g_m$) reduces the stage gain and isolation between the input and output of the cascode. These tradeoffs resulted in the circuit of Figure 2 which is shown simplified and biased in Figure 5. Later simulations showed that this topology gave adequate power gain and acceptable gain ripple when shunt/shunt negative feedback was applied around the first buffered cascode stage of this two stage buffered cascode IF amplifier.

SIMULATION and RESULTS

As indicated above, the two stage buffered cascode IF amplifier of Figure 5 was simulated using MicroSim's 7.1 Release Pspice evaluation software running on a Pentium-Pro processor. The following table lists the tests performed on this circuit

IF Amp Simulations

Type	Result
DC/Bias	various I_D, V_{DS}, V_{GS}. P_{DISS} found from this
AC sweep*	A_v vs. Frequency, Z_{IN}, Z_O, S_{22} ($gamma_{out}$)
Transient+	V_O vs. time and examination of waveshape at 10 mW into 75 ohms

* 0.950 GHz-1.450 GHz
+ 1.200 GHz

A. DC/Bias.

Figure 5 shows a sampling of bias currents and voltages. All transistors were in saturation (i.e., linear region) operation. P_{DISS} can be found from this figure to be

$$P_{DISS} \sim (22 + 2 + 32)\text{mA X } 2 \text{ X } 15\text{V} \sim 1.7 \text{ W}$$

which is fairly hefty dissipation. The output buffer must deliver about 16 mA peak into 75 ohms to ensure a P_L of 10 mW. Thus, for nominally linear operation, I_{DQ} must be at least 16 mA. A rule of thumb for good linearity is to demand no more than 10% of I_{DQ} into the load on peaks. Obviously, an I_{DQ} or 160 mA is impossible with these devices and, of course, dissipation would be quite excessive. A value of I_{DQ} for the buffers of ~ 32 mA was a compromise between dissipation and linearity.

The ~ 24 mA I_{DQ} of the 300 micron CS devices was chosen to help ensure that the g_m of these devices was sufficiently high to obtain good gain.

(Perhaps the inter-stage buffer might have been designed for less I_{DQ} since its power out requirement is significantly less than that for the output buffer.)

B. AC Analysis.

1. Gain

Figure 6 shows a plot of A_{vdB} (which is a good approximation of P_{dB} as shown above) versus frequency. The gain was ~ 47.3+/-0.3 dB which exceeded the original ripple specification of +/-0.5 dB.

2. Z_{IN}.

For this test the output was terminated in 75 ohms and a current source of 1A was connected to the input. Thus, Z_{IN} was equivalent to V_{IN} (i.e., the voltage across the 1A test source). Figure 7 shows Z_{IN} versus frequency. At these frequencies, $|Z_{IN}|$ was low (~ 70 ohms) and inductive.

3. Z_O.

The same test was performed at the output as for Z_{IN}. Figure 8 shows the results. $|Z_O|$ was nominally 200 ohms and inductive. For this test, 0.17 nH of bondwire inductance was placed in series with V_{DD} (multiple pads for V_{DD} and ground placed several bond wires in parallel) and 0.5 nH was placed in series with the output.

4. S_{22}/$gamma_{out}$.

The test circuit of Figure 9 was used to obtain S_{22} for this circuit. Figure 10 shows S_{22} versus frequency. A midband value of ~ 0.53 gives a rather high SWR_{OUT} of 3.3 .

C. Transient Analysis.

A transient analysis was performed at 1.2 GHz with an input of 5.5 mV. In order to obtain a fine enough time step (which this simulation software chose automatically), a small source of 1 uV at 5 GHz was placed in series with the 5.5 mV source. Figure 11 shows the results of this test. The ~1.2 V_P output gave

$$P_O = 1.2^2/(2*75) = 10 \text{ mW}$$

into 75 ohms as required. Visual inspection of the waveshape indicates only small harmonic content (some compression did occur on the positive peaks). The bias current and V_{OQ} of the output buffer was chosen to ensure that 1.2 V_P could be obtained from the output without severe compression or clipping.

LAYOUT

A. General Information.

The IF amplifier of this project was laid-out manually in the MDS environment using the TQS HA2 layout subcircuits as templates obtained from the TQS file tqha2fv2.sf. (The layer definitions contained in this file appear in Figure 12 and a list of the layout subcircuits provided in this file appears in Figure 13.) The reader is referred to the ABSTRACT where all layout subcircuits for the IF amp are listed along with their derivation. Once these subcircuits were created, a layout workbench/drawing was made using a page resolution of 1000 data base units (dbu) per micron and a snap grid spacing of 0.5 micron (as it turns out, the design rule check at TQS may be more easily passed if a snap grid spacing of 1 micron is chosen). TQS's element placement rules, which amount to minimum spacing rules, appear in Figures 14 and 15. The layers called metal0 and metal1 were used for all interconnection of circuit elements which was carried out using the insertion of rectangles. Where required, connection between metal0 and metal1 was made using the layer called via1. For example, in the layout subcircuit called fet300, the multiple source regions were ganged together using both metal0 and metal1 to create the overall source electrode for connection to other elements. Finally, Figure 16 shows the layer names, colors, patterns, etc., used for the layout subcircuits and the final layout of the IF amp.

B. MDS Commands for Layout Generation.

Various commands that allow efficient layout generation in MDS include:

1. "Layout": This command is invoked by clicking it on the MDS Simplified User Interface (SUI) palette to begin a new layout.

2. *SET/GRID*: This command allows the user to set the page resolution as the number of data base units (dbu) per unit length. For this project (and upon TQS's requirements as it turned out) the resolution was set to 1000 dbu per micron. One may also set the grid spacing under this command (a 1 micron snap grid is recommended).

3. *PERFORM/SHOW/DISTANCE/POINT TO POINT*: This command (along with mouse clicks) shows the linear distance between selected points on the drawing. Clicking the window border button WD erases the measurements.

4. *PERFORM/IDENTIFY*: Selecting a layer and invoking this command will cause the MDS message box to open and display the identity of the layer (per the imported TQS layer definition file, of course).

5. *PERFORM/ASSOCIATE/MERGE*: This command removes the distinction between individual layer rectangles that were drawn during the course of interconnection, for example.

6. *PERFORM/EXPORT/GDS-II FILE/FLATTEN*: This command writes the GDSII file for the layout which, for this project, was submitted to TQS for Design Rule Check (DRC). Selecting 'FLATTEN' results in the removal of the original distinction that existed between the layout subcircuits and the interconnects.

7. *PERFORM/IMPORT/GDS-II FILE*: This command performs a file read of a GDSII layout file for import into the MDS environment. It was noted that this command was accessible only from a layout drawing page (a dummy layout page was created for this purpose). MDS prompts the user for the name of the layout file as well as asking for the name of the layout file where the layer definitions are found (which in turn must be located in the file or workbench where the IMPORT command was issued from). The end result of this command is an automatically created layout drawing which has the same name as that of the GDSII file.

8. *SET/LAYER/VISIBLE-ON or -OFF*: This command controls layer visibility on the layout drawing page.

9. *INSERT/LAYOUT SUBCIRCUIT/BY LABEL*: This command is used to pick and place the individual layout subcircuits within the final layout drawing.

10. *INSERT/RECTANGLE*: (Also found as a drawing window border button-IR.) This command along with clicking and dragging draws rectangular shapes in the layer selected (which are delineated by color and/or texture). This command is essential for custom layout subcircuit creation and interconnection on the final layout.

11. *INSERT/CONSTRUCTION LINE*: This command inserts a guide line across the whole drawing for reference when placing subcircuits and rectangles on the final layout.

12. *STRETCH*: This command allows the user to enlarge or shrink layout features (e.g., rectangles, parts of subcircuits or whole subcircuit dimensions) once the appropriate edges or vertices of the feature are selected. This command allows the resizing of TQS layout subcircuits directly for the purpose of creating custom layout subcircuits.

13. *TOOLS/LAYER DIALOG*: This command opens a dialogue box that contains all the process layer names. If one wishes to insert a rectangle as a metal1 interconnect between, for example, the 300 micron dFET source and the top plate of an HA2 MIM capacitor, then metal1 is selected in the layer dialogue box for such an edit to the layout. This box, when used with SET/LAYER/VISIBLE/OFF, allows the user to show a single layer at a time which is especially useful when laying down interconnects.

C. TQS Layout Subcircuits Referenced for IF Amplifier.

The following table lists the TQS HA2 layout subcircuits used as a template/reference for building a custom layout subcircuit or modified directly by stretching. (Also see table in ABSTRACT section above.)

TQS HA2 Subcircuits Referenced for IF Amp Layout Subcircuits

TQS Subcircuit	Description
pdhss50	0.5 um X 50 um symmetric dFET
pbf 510	6 fingered (X50 um) interdigitated GaAsFET
ps15p15	N+ overlap diode
rn10	10 um X 10 um thin film nichrome resistor, 50 ohms/sqr.
pcap50	50 um X 50 um MIM capacitor, 0.590 fF/um^2
ppad100	100 um X 100 um bondpad (used unmodified)

Figure 17 give a pictorial of a dFET, MIM cap and NiCr circuit as fabricated on the wafer surface for the TQS HA2 process.

D. IF Amp Layout Subcircuits.

The following table lists the layout subcircuits specifically required for the DBS IF amplifier designed for this project.

HA2 Layout Subcircuits Used In the Layout of DBS IF Amp

Subcircuit/Name	Purpose
6 finger X 50 um interdigitated dFET/fet300	CS device of cascode stage
4 finger X 50 um interdigitated dFET/fet200	buffer devices
1 finger X 20 um dFET/fet20	CG device of cascode stage, biasing
150 um N+ overlap diode/diode150	biasing
130 um X 130 um 10pF MIM capacitor/cap10	AC coupling and bypass
500, 2000, 3500, 4000, 10000 ohm nichrome thin film resistors/rn500, rn2000, etc.	biasing and feedback

E. Creating the IF Amp Custom Layout Subcircuits.

1. fet300,fet200.

The TQS layout subcircuit pbf 510 could not be used directly due to its inclusion of, what amounted to, pads in metal0, metal1 and air bridge. Therefore, fet300 was built by placing six pdhss50 symmetric dFET "fingers" side by side, connecting alternating drain/source regions together with metal0 and ganging the source metal0 blocks together with an overlay of metal1 connected through via1 regions. The drain metal0 blocks were ganged directly by bringing a metal0 region out. The individual metal0 gate pads were also brought out as a larger metal0 region for interconnect purposes. All this was done using the original TQS pbf510 spacings as a template or reference. The fet200 IF amp layout subcircuit was merely a pared down version of the fet300 subcircuit. Commands 2, 3, 8, 10 and 13 (above) were most useful in this procedure. Figure 18 shows the layout of fet300 (fet200 is completely analogous).

2. fet20.

A single pdhss50 symmetric dFET was used to create the fet20 by merely “stretching” the layout down to a width of 20 microns using the command of that name. Metal0 was used for all three electrodes (drain, source and gate) for interconnection.

3. diode150.

Again, a TQS original layout subcircuit, in this case the ps15p15 N+ overlap diode, was stretched to obtain a width of 150 microns. Both the anode and the cathode were built of metal0. Figure 19 gives the layout design rules for this device.

4. cap10.

A TQS pcap50 layout subcircuit was stretched to obtain the 10 pF of capacitance. Figure 17 shows the assembly of a TQS MIM cap. The capacitance for this technology is given as 0.6 fF/um2, thus, pcap50 was stretched to form a 130 um X 130 um square to give 10 pF of capacitance for coupling and bypass. The bottom plate of cap10 is composed of metal0 and the top plate is made of metal1 (the MIM layer provides the precise area which the capacity is based on).

5. rn500, etc.

TQS’s rn10 was stretched (and meandered) to form the five different resistor values needed for this IF amp. Figure 20 shows the layout for a thin film NiCr resistor in HA2. A square can be considered to be 10 um X 10 um which has a resistance of 50 ohms. From this fact one is able to closely approximate the required resistor length.

F. Final IF Amp Layout.

The circuit of Figure 2 was laid out using the layout subcircuits just described within the MDS environment. Much of the interconnection (performed by inserting rectangles and a few triangles with 45^{o} hypotenuses) was done in metal0. Where necessary or reasonable, metal1 was used (e.g., places where two “wires” crossed). Any connection required between metal0 and metal1 was accomplished using via1. Figure 21 shows the silhouette of the final DBS IF amp layout. Five 100 um X 100 um bond pads at the top supply the 15V, the top left pad is V_{IN}, the top right pad is V_{OUT} and the bottom seven pads are ground. Since simulation showed that supply inductance severely affected the performance of the amp, as many pads as possible were employed to reduce the total inductance. All pads were spaced at least 50 um apart. A GDSII file was sent to TQS where, with minor adjustments, the layout passed DRC. Layout Versus Schematic (LVS) is pending at the time of this writing. The overall layout dimensions are 1293 um X 1038 um (1.3 mm X 1.0 mm).

CONCLUSION

This project saw the design, simulation, layout and DRC of a two stage, buffered DBS IF amp. Reasons for the topology chosen, bias quantities and layout strategy have been offered. Simulation results and the means and method of the layout have also been given. This project proved interesting and challenging especially in the area of layout since it had never before been done by the writer. It is believed that fabrication (at TQS) and testing will follow at some point in the future.

FIGURES