EE 532 PROJECT

Design of an IF Amplifier

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1   Introduction

This project involves the design of an IF amplifier with given specs. At the first stage, an amplifier topology has been chosen and preliminary calculations have been performed. Then the component values have been optimized by simulating the design in PSPICE. As the last step, layout for the amplifier has been generated using HP-MDS tool.

Specifications for the amplifier is given as follows:

- Bandwidth : 950MHz - 1.45 GHz

- Gain : Min. 45 dB over the specified frequency range

- Ripple : Max. $\pm 0.5 dB$ within the bandwidth

- Output power : 30 dBm on 75Ω load

- Output SWR : 1.2 (75Ω system)

- Supply : Max. 15V, single supply

Design goal was first to satisfy the requirements listed above, then try to optimize noise, power consumption, third-order intercept point and sensitivity. In the following sections, design steps are explained and the results are discussed.

2   Amplifier Design and Simulation

The amplifier has been designed using Triquint's HA2 GaAs MESFET technology. For simple hand analysis and further simulation, operation of the MESFET devices are characterized by TOM2 model equations, where TOM2 stands for the second generation Triquint's Own Model. A typical MESFET transistor is depicted in Fig. 1.
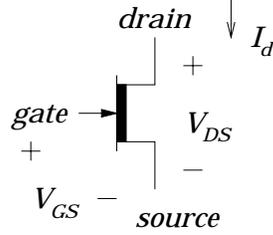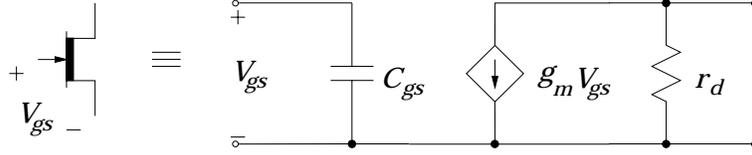

Figure 1: GaAs MESFET Transistor

Figure 2: Simplified small signal equivalent circuit of a MESFET

Basic MESFET equations are given as follows:

$$I_d \cong \beta W (V_{gs} - V_t)^2 \frac{\alpha V_{ds}}{\sqrt{1 + (\alpha V_{ds})^2}} \ , \ V_t = V_{to} - \gamma V_{ds} \tag{1}$$

$$I_d \cong \beta W (V_{gs} - V_t)^2 \ , \ V_{ds} >> \frac{1}{\alpha} \ \ (Saturation) \tag{2}$$

$$V_{gs} \cong \sqrt{\frac{I_d}{\beta W}} + V_t \tag{3}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \cong 2\beta W (V_{gs} - V_t) = 2\sqrt{\beta W I_d} \tag{4}$$

$$r_d = \frac{\partial V_{ds}}{\partial I_d} \cong \frac{1}{\gamma g_m} \cong \frac{V_{gs} - V_t}{2\gamma I_d} \tag{5}$$

In order to obtain the approximate behaviour of the circuit, a simple AC equivalent model is used. Figure 2 shows the small signal circuit of a MESFET.

Several amplifier configurations have been reported in the literature. As the basic block, we have chosen g_m-enhanced cascode amplifier [1], as shown in Fig. 3. This circuit is the modified version of conventional cascode amplifiers. Two main factors leaded us to use this circuit topology: Bandwith and gain.
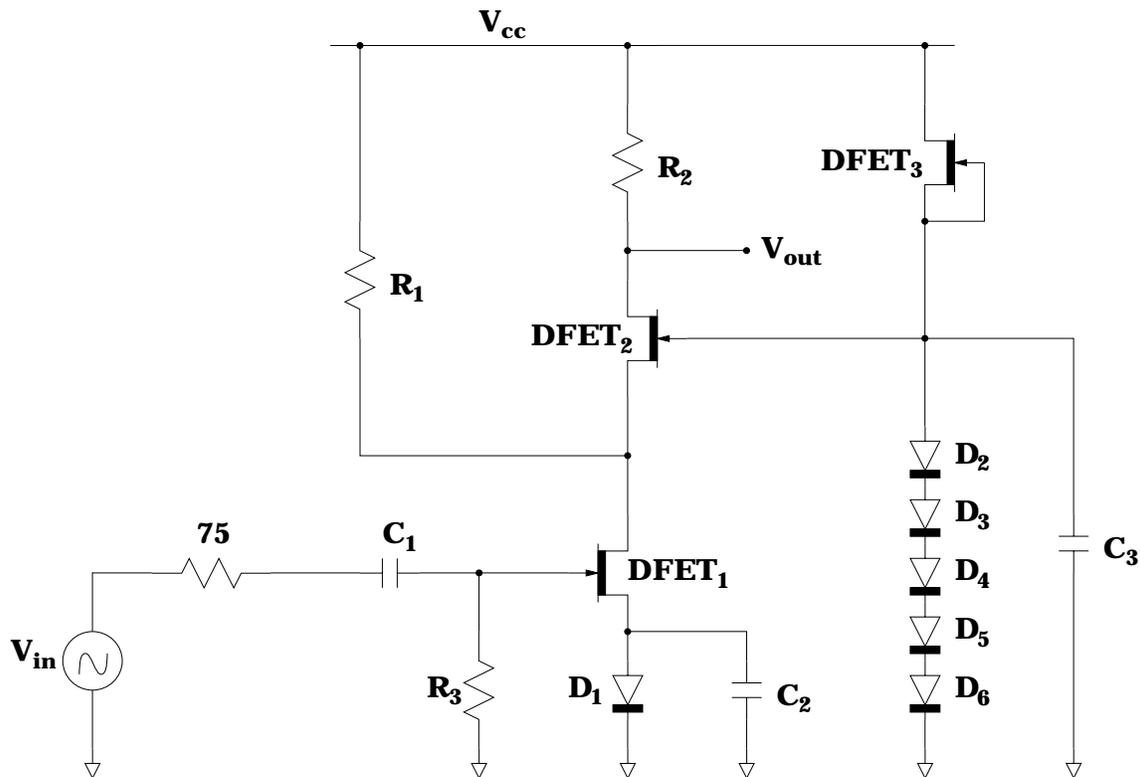

Figure 3: g_m-enhanced cascode amplifier

The main limitation on the bandwidth of an amplifier is the gate-to-drain capacitance of the input FET device. In order to obtain a reasonably high gain, a large MESFET device has to be used at the input of the amplifier. Due to Miller effect, even a very small capacitance (in the order of femto-farads) deteriorates the bandwidth of the amplifier because of the high voltage swing on that capacitor. Cascode stages do not suffer this Miller effect, therefore high gain can be achieved over a wide range of frequencies.

As its name suggests, the g_m-enhanced cascode configuration enables us to choose large g_m values for the input transistor ($DFET_1$) due to the resistive path from V_{cc} to the drain of $DFET_1$. By inspection, gain for this stage can be found to be proportional to g_{m1} and R_2, where g_{m1} is the transconductance of the $DFET_1$ and R_2 can be considered as the load resistor. Without the resistor R_1, I_{d1} for $DFET_1$ cannot be chosen high enough (a few tens

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of milli-Amps) since it causes too much voltage drop on a large R_2 (in the order of a few $k\Omega$). For proper operation, all transistors should be well above the knee, which means that their V_{ds} should be above $3 - 4$ volts. Keeping both I_d and R_2 high can be accomplished by supplying the drain current for $DFET_1$ via R_1.

When the transistor $DFET_1$ is biased with a zero gate-to-source voltage, I_{dss} becomes too large (around 60mA for the transistor with $W = 300\mu$), which requires either R_1 and R_2 or W_1 to be smaller, causing the gain to decrease. Once the current value is set to its maximum possible value, larger width for the transistor provides larger transconductance value, which can be achieved by choosing a negative V_{gs} value. The simplest way to do that is to connect a diode from source to ground. In addition, A by-pass capacitor is connected in parallel to the diode to decrease emitter degeneration due to finite diode resistance. A small FET is chosen for the common-gate $DFET_2$ since it conducts a small current. Gate bias of $DFET_2$ is performed by using a diode-connected DFET and 5 diodes in series. To obtain ac ground at the gate of $DFET_2$, a by-pass capacitor is connected in parallel to the diode string.

In addition to these, a coupling capacitor is placed between gate and the input signal since the amplifier is AC coupled. In order to bias the input FET ($DFET_1$) properly, a large resistor is connected between its gate and ground.

To calculate the approximate gain, small signal model for the g_m enhanced cascode amplifier is drawn as shown in Fig. 4.
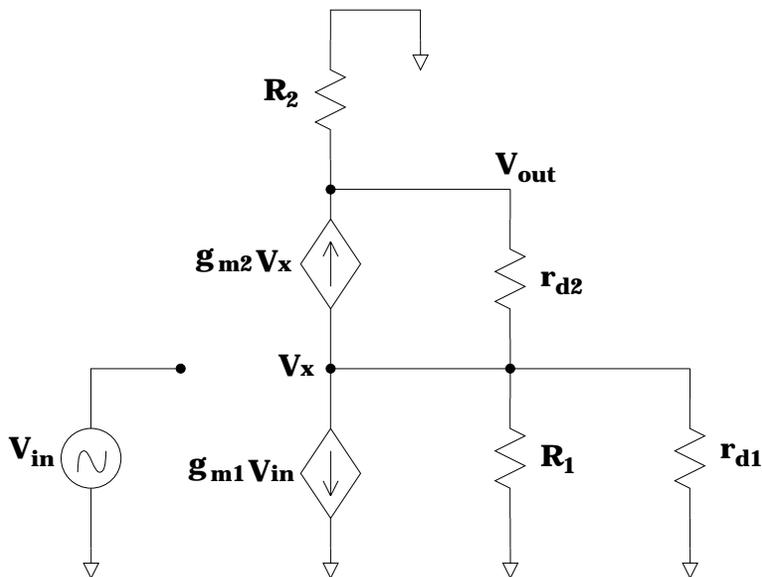

Figure 4: Small signal circuit for the amplifier

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KCL at circuit nodes yields

$$g_{m1}V_{in} + V_x G_1 + V_x g_{d1} + g_{m2}V_x + (V_x - V_{out})g_{d2} = 0 \tag{6}$$

$$V_{out}G_2 - g_{m2}V_x + (V_o - V_x)g_{d2} = 0 \tag{7}$$

resulting in

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}(g_{m2} + g_{d2})}{(G_2 + g_{d2})(G_1 + g_{d1}) + G_2(g_{m2} + g_{d2})} \tag{8}$$

where

$$G_1 = 1/R_1 \tag{9}$$
$$G_2 = 1/R_2 \tag{10}$$
$$g_{d1} = 1/r_{d1} \tag{11}$$
$$g_{d2} = 1/r_{d2} \tag{12}$$

Rearranging the terms, we can obtain an alternative equation for the gain:

$$\frac{V_{out}}{V_{in}} = -\frac{1 + \gamma}{\gamma^2 + \frac{1+\gamma}{g_{m1}R_2} + \frac{\gamma}{g_{m1}R_1} + \frac{\gamma}{g_{m2}R_2} + \frac{1}{g_{m1}g_{m2}R_1R_2}} \tag{13}$$

By close inspection on Eq. 13, we can see that the dominant term in the denominator is $\frac{1+\gamma}{g_{m1}R_2}$, where γ is given as 0.076. The next step is to choose the component values and get a reasonable gain from the amplifier. Since we had the transistors with $W = 300\mu$ in the device library, we have started the design by choosing $W_1 = 300\mu$. For $DFET_2$, we have chosen $W = 20$, since it conducts a small current when compared to $DFET_1$. I have tried to maximize gain by sweeping the resistance values in MATLAB, and obtained the initial values for them.

Using the g_m-enhanced cascode amplifier as the basic block, we have designed the two-stage amplifier as shown in Fig. 5 with some modifications and additions. In order to get a flat magnitude characteristics within the specified frequency range, a local feedback is required in the first stage. Due to excess phase shift, we could not apply a global feedback from the output of the second stage to the input stage. To reduce the effect of feedback loading on the amplifier gain, we have inserted a buffer at the output of the first stage, which is followed by the second stage via a coupling capacitor. We put another buffer to the output to decrease the output impedance, and hence the output SWR. Common gate transistors in both stages are biased by the same diode string.
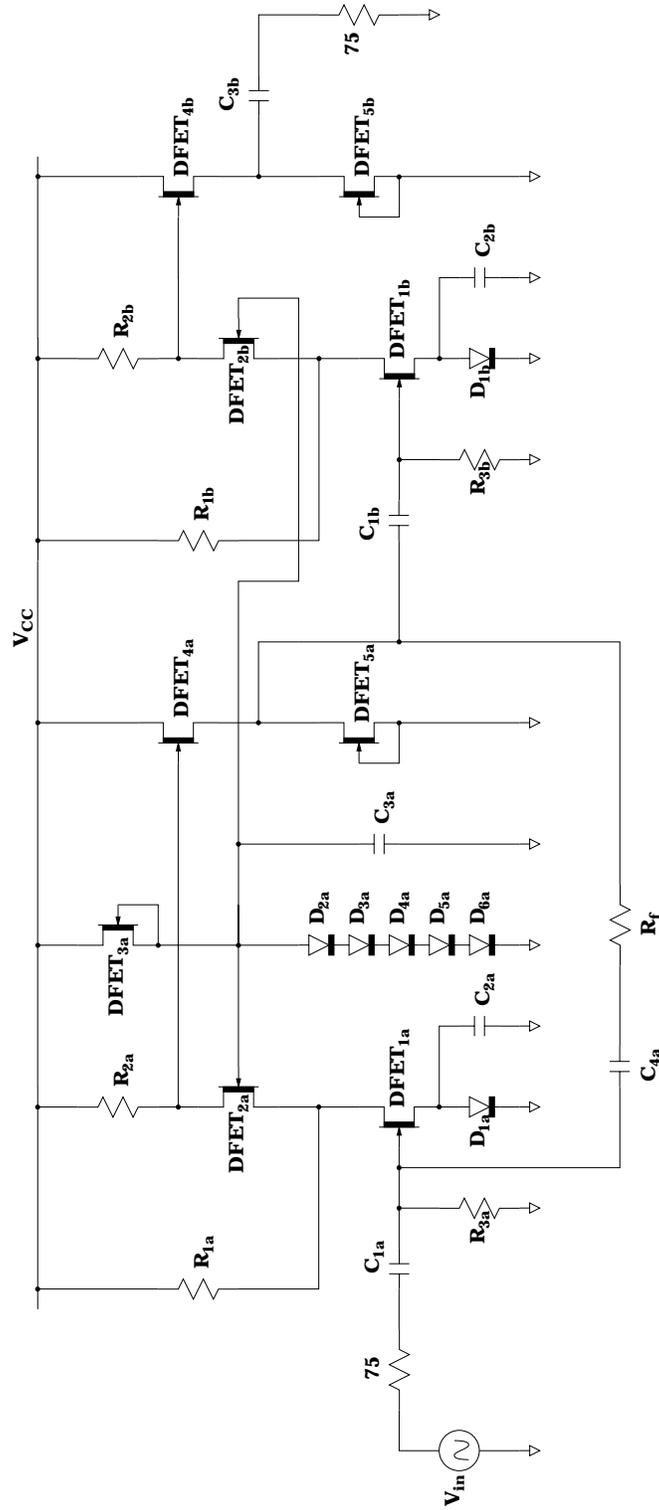
Figure 5: Complete amplifier schematics

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Another specification for the design was to get $s_{22} < 0.2$. To achieve this, we have chosen large transistors for the output buffer. However, as the size of transistors get larger, our frequency response gets worse. Therefore, output SWR has been compromised for a better frequency response.

We have used PSPICE in order to simulate and optimize the circuit in Fig. 5. After we obtained the best values to satisfy the requirements, we inserted bondwire inductances (0.5nH for each pad) to the circuit. Since connecting inductors in parallel decreases the overall inductor, we have assumed 10 pads for the supply and ground connections. With the previous circuit parameters, addition of inductors caused an overshoot in the frequency characteristics. We have tried to eliminate this by reducing R_f and R_2 for the second stage. Simulation results and circuit schematics with bias points are included in the Appendix.

3   MDS Setup for Triquint HA2 Process

In order to draw the layout for the amplifier, I have used the layout tool of HP-MDS. Default technology (i.e. layer definitions) of MDS is different from HA2 process, therefore it has to be configured in order to use the HA2 techology. Appropriate technology files should be imported into MDS to change layer definitions.

Two files are required to set up MDS for Triquint HA2 process. First one is named **process_ha2**, which contains layer information. The second file is a gdsII stream named **tqha2fv2.sf**, which consists of HA2 cell layouts. Configuration steps are explained as follows:

- Start MDS and open a new file.

- Create a new workbench within the new file.

- Create a layout named **layers** in the new workbench.

- Open the layout and change page to the index page.

- Using mouse, **insert - layer page**, drop the rectangle beneath drawing page listing.

- Change page to drawing page, and **perform - import - EGS archive file - process file only**.

- In the dialog box, enter the full pathname for the layer file named **process_ha2**, enter **Y** for the next dialog box.

- From the drawing page, **perform - import - gdsII file**.

- In the dialog box, enter the full pathname for the gdsII file for cell layouts, named

Layer Name	Layer ID
iso_imp	6
n_minus_imp	1
n_plus_imp	2
NiCr	3
ohmic	5
gate_metal	7
metal0	9
MIM	23
metal1	15
via1	14
air_bridge_post	10
air_bridge	11
passivation_via	12
backside_via	20
backside_via_coat	21

Table 1: Triquint HA2 Process Layers

tqha2fv2.sf. For the next dialog box, enter **layers** for the icon name with the new layer definitions.

Once these steps are completed, cell library can be used to draw the amplifier layout. Unfortunately, HA2 design rule file for MDS is not available. The only existing DRC file is the one for ICED, which is the layout tool used by Triquint. However, since we have the HA2 cell library (layout blocks) and documented layout rules, an error free layout can be drawn by careful design.

4 Triquint's HA2 Technology O er iew

HA2 is a high performance GaAs D-MESFET based process which is useful for a wide variety of low noise and medium power applications. List of layers for HA2 process are shown in Table 1. Three interconnect layers can be used to perform routing: Metal0, metal1 and air bridge. Via1 layer is used to connect metal0 and metal1. Air bridge is connected to metal1 layer by using air bridge posts, which also serve as a support for the floating metal layer. A typical cross-section of HA2 layers are depicted in Fig. 1.

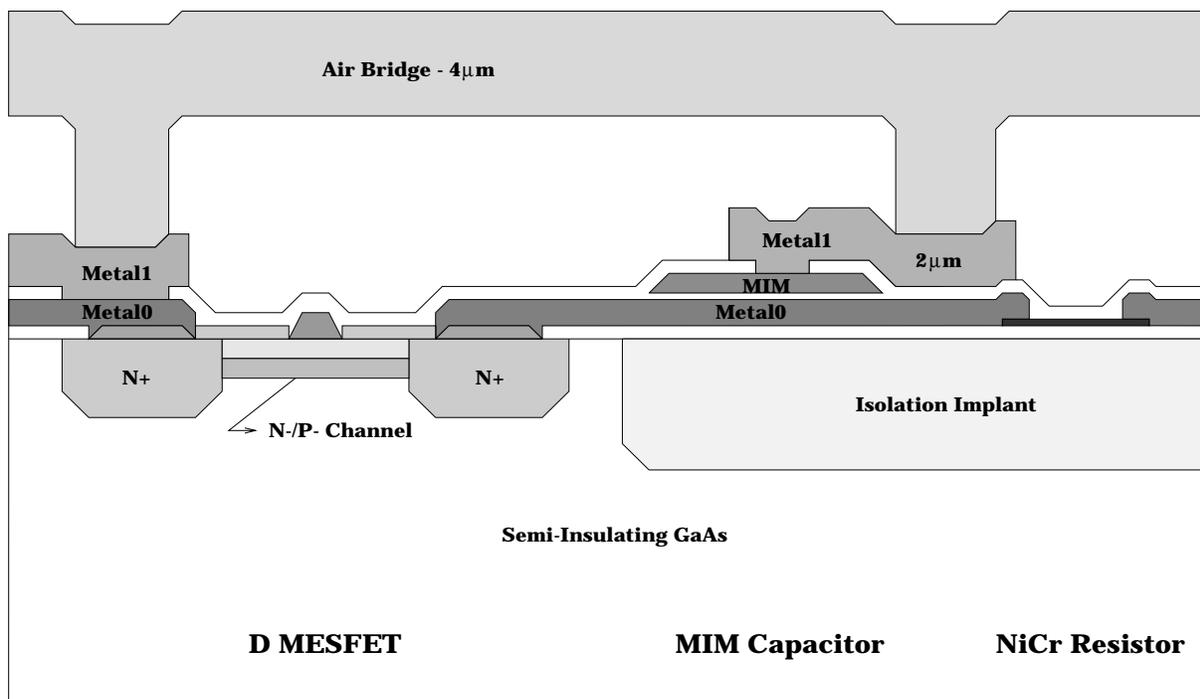Process parameters for HA2 technology are summarized in Table 2.

Air Bridge - 4μm

Metal1

Metal1   2μm

MIM

Metal0   Metal0

N+   N+

Isolation Implant

N-/P- Channel

Semi-Insulating GaAs

D MESFET   MIM Capacitor   NiCr Resistor

Figure 6: Cross-sectional view of HA2 layers

Parameter	Nominal Value
D-Mode Pinchoff Voltage	$-1.70\ V$
D I_{dss}, $V_{ds} = 4.0\ V$	$170\ \mu A/\mu m$
D Cutoff Frequency ($F_t\ H_{21},\ I_{dss}$)	$19\ GHz$
D F_{max} (Unity Power Gain, Matched)	$\sim\ 60\ GHz$
D Transconductance	$135\ mS/mm$
D Breakdown	$16\ V$
Thin Film Resistor Sheet Resistance	$50\ \Omega/square$
D Implant Resistor Sheet Resistance	$1000\ \Omega/square$
MIM Capacitance per Area	$0.6\ fF/\mu m^2$
Metal0 Sheet Resistance ($0.5\mu m$ thick)	$110\ \Omega/square$
Metal1 Sheet Resistance ($2\mu m$ thick)	$10\ \Omega/square$
Airbridge Sheet Resistance ($4\mu m$ thick)	$5.5\ \Omega/square$

Table 2: HA2 Key Parameters

5   Layout Generation

For a high-performance analog circuit layout, full-custom design methodology is essential. Placement and routing of the blocks should be performed carefully to minimize the chip area, possible crosstalk and parasitic capacitors. Furthermore, the design can be optimized for better component matching and temperature stability.

Some important points for drawing the layout are listed below

- Grid should be set correctly. Select **set - grid** and complete the form as follows:
  Current page resolution : **1000** dbu per **um**
  Major grid spacing : **10** um
  Minor grid spacing : **1** um
  Snap grid spacing : **1** um
  Grid visibility : **ON**
  Snap to grid : **ON**

- Try to use rectangle shapes instead of polygons, if possible. If you draw polygons, use orthogonal (0° or 90°) or diagonal (45°) angles for the polygon edges.

- Use hierarchy in the design, i.e. insert layout blocks and route them at the top level of hierarchy. Try to modify the existing layout library instead of drawing them from scratch, if needed. This will help to minimize the possibility of DRC errors in the layout.

- If some shapes in layout blocks are on 0.5μ grid (as the metal2 layer in capacitor), either temporarily switch to 0.5μ grid spacing, or stretch your connection rectangles by 0.5μ using **stretch - to specific point - relative x,y**. Never place a via1 shape on a 0.5μ grid.

- After drawing the layout, check the connectivity of each layer separately. You can **set - layer - visible-off - all** and then set any of them as the visible layer. Make sure that only one layer is visible during the check.

In order to minimize DRC errors, I have either used the components in the cell library, or slightly modified them by stretching. In MDS layout tool, corner points of the rectangles and polygons can be selected by mouse (clicking the left mouse button and dragging it while pressed). Then, using STRETCH command the figure can be stretched in any direction.

Furthermore, I have not used the minimum requirements for the design rules, which generally has to be done for minimum chip area. In order to have an error free layout, I have kept the distances and sizes more than necessary, which caused the chip area to be slightly larger. The layout I have drawn has been found to be DRC error free. It has also passed the LVS (layout versus schematics) test, and now ready for fabrication. Consequently, a successful layout can be produced in the absence of design rule checking and LVS tools, with

Element Type	Cell Name	Description
Symmetric DFET	pdhss50	0.5×50 dfet
Diode	ps15pl5	3×5 N+ overlap diode
Resistor	rn10	10×10 thin film resistor
Capacitor	pcap50	50×50 MIM capacitor
Pad	ppad100	100 sq. bond pad

Table 3: Devices used from HA2 Device Library

a little more time and chip area spent as the price.

Table 3 shows the list of components that I have used in my layout. These components were extracted from the gdsII input file **tqha2fv2.sf**.

6   Conclusion

We have designed an IF amplifier with the given specs. Results for the final amplifier are summarized as follows:

- Bandwidth : 950MHz - 1.45GHz

- Gain : 47-48 dB

- Ripple : 0.99dB

- Output Power : $30 dBm$ on 75Ω load

- Supply Voltage : 15V, single

- Output SWR : 2.5 - 6 (within the frequency range)

Consequently, we have satisfied most specifications, except for the output SWR. It can be decreased by increasing the size of transistors in the output buffer, however this degrades the frequency characteristics, which, we have assumed that, is more important than output SWR. Other than that, the amplifier operates successfully and its layout is ready for fabrication.

References

[1] S. S. Taylor and T. P. Thomas, "A $2pA/\sqrt{Hz}$ $622Mb/s$ GaAs MESFET Transimpedance Amplifier," *IEEE International Solid-State Circuits Conference*, pp. 254–255, 1994.

[2] N. Scheinberg, R. J. Bayruns, and T. M. Laverick, "Monolithic GaAs Transimpedance Amplifiers for Fiber-Optic Receivers," *IEEE Jornal of Solid State Circuits*, vol. 26, no. 12, pp.1834–1839, Dec. 1991.

[3] TriQuint Semiconductor HA2 Design Manual

[4] HP-MDS Design Manual