TOM-2: An Improved Model for GaAs MESFETs

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Abstract

This report describes an improved MESFET model developed at TriQuint Semiconductor, Inc. The model, designated TOM-2 is an incremental improvement based on TriQuint's original TOM[1] model[4].

This document is intended as an aid to workers who wish to implement TOM-2 in a specific simulator. It provides a complete mathematical description of the model. It is not intended as end user documentation.

[1] **T**riQuint's **O**wn **M**odel

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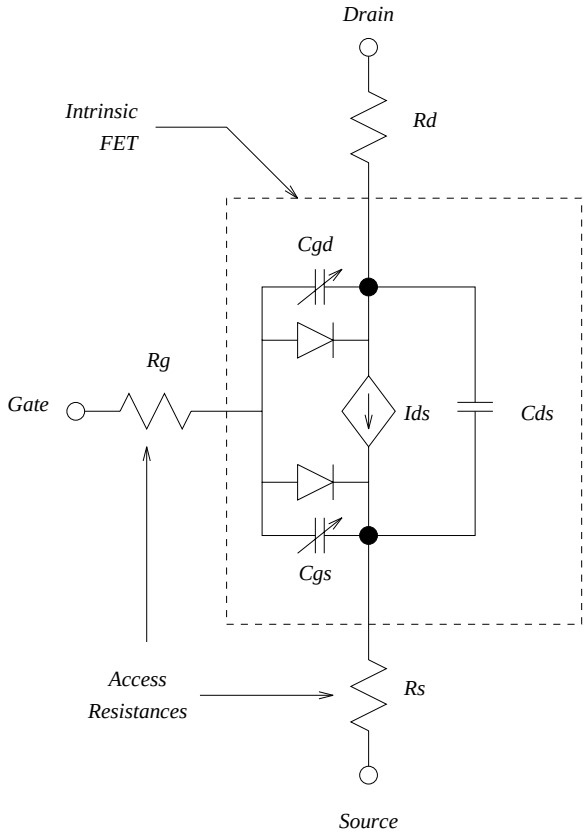
Figure 1: TOM-2 Model.



1 Introduction

TOM-2 is an improved model for GaAs MESFETs. It is based on the original Triquint model (aka. TOM, herein referred to as TOM-1) with refinements to improve accuracy in the knee and subthreshold region. Particular attention was given to the temperature effects.

The model has been implemented using Pspice version 6.1 but should be readily portable to other analog simulators.

This model does not claim to be the final word in MESFET models—it is simply a next order effort to improve the overall accuracy of the model based on several years of experience with TOM-1. TOM-2 retains the desirable

features of TOM-1 while improving performance in the subthreshold (V_{gs}) near cut-off, and knee regions (V_{ds} of 1 volt or less). Additional temperature coefficients are included related to the drain current, and major deficiencies in the behavior of the capacitance as a function of temperature are corrected.

2 Equivalent Circuit

Figure 1 shows the basic model used in TOM-2. The model details specify how the current sources and the variable capacitors depend on bias conditions and on temperature.

The equations given in the rest of this document reference the voltages across the "intrinsic" portion of the FET as outlined in the figure. These intrinsic voltages are denoted as V_{gs} and V_{ds} for the gate-to-source and drain-to-source respectively.

Note that the model does not provide a mechanism for modeling the low frequency drain conductance dispersion that is well known in GaAs MESFETs. We model this effect with an external subcircuit with feedback coupled through a low pass RC network (not described in this document).

3 Basic Equations

3.1 Current source equations

The following expression is used to compute I_{ds} for the current source in figure 1.

$$I_{ds} = \frac{I_{dso}}{1 + \delta V_{ds} I_{dso}} \tag{1}$$

Where:

$$I_{dso} = w\beta V_g^{Q} \cdot \mathrm{F}_d(\alpha V_{ds}) \tag{2}$$

$$F_d(x) = \frac{x}{\sqrt{1+x^2}} \tag{3}$$

and V_g is given by:

$$V_g = QV_{st} \ln\left[\exp\left(\frac{V_{gs} - V_{to} + \gamma V_{ds}}{QV_{st}}\right) + 1\right] \tag{4}$$

where V_{to} and γ are constants. w is the device width.

In general, we expect V_{st} to be near the thermal voltage kT/q, or about 0.026 mV at 25C. This leads us to present the V_{st} by an ideality factor, N_{st} thus:

$$V_{st} = N_{st}\left(\frac{kT}{q}\right) \tag{5}$$

In addition, it is observed that the subthreshold slope varies slightly with V_{ds}, so we put in a linear dependence to account for this:

$$N_{st} = N_g + N_d V_{ds} \tag{6}$$

Notice that $N_{st} = 0$ corresponds to no subthreshold—that is, the current cuts off sharply at threshold. This behavior is similar to a diode where setting the ideality factor equal to zero results in a piecewise linear behavior.

The gate current, I_g is the sum of the current flowing in the gate-drain diode, I_{ds}, and the gate-source diode, I_{gs}. These currents are given by the classical diode formula:

$$\begin{aligned} I_g &= I_{gs} + I_{gd} && (7)\\ I_{gs} &= wI_s(e^{qV_{gs}/nkT} - 1) && (8)\\ I_{gd} &= wI_s(e^{q(V_{gs}-V_{ds})/nkT} - 1) && (9) \end{aligned}$$

Notice also that the total drain current, I_d includes a component flowing from the gate:

$$I_d = I_{ds} - I_{gd} \tag{10}$$

Usually, the above equations will be are incorporated into a subroutine that must deliver the currents I_d and I_g back to the simulation engine.

3.2 Capacitance Equations

The Capacitance equations are based on those proposed by Statz, et. al.[8].

$$\begin{aligned} C_{gs} &= \frac{C_{gso}}{\sqrt{1-\frac{V_n}{V_{bi}}}}\frac{1}{2}\left\{1+\frac{V_{eff}-V_{to}}{\sqrt{(V_{eff}-V_{to})^2+V_\delta^2}}\right\} \\ &\quad \times\frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \\ &\quad + C_{gdo}\frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \qquad (11) \\ C_{gd} &= \frac{C_{gso}}{\sqrt{1-\frac{V_n}{V_{bi}}}}\frac{1}{2}\left\{1+\frac{V_{eff}-V_{to}}{\sqrt{(V_{eff}-V_{to})^2+V_\delta^2}}\right\} \\ &\quad \times\frac{1}{2}\left\{1-\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \\ &\quad + C_{gdo}\frac{1}{2}\left\{1+\frac{V_{gs}-V_{gd}}{\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}}\right\} \qquad (12) \end{aligned}$$

where:

$$\begin{aligned} V_{eff} &= \frac{1}{2}(V_{gs}+V_{gd}+\sqrt{(V_{gs}-V_{gd})^2+\left(\frac{1}{\alpha}\right)^2}) \\ V_n &= \frac{1}{2}(V_{eff}+V_{to}+\sqrt{(V_{eff}-V_{to})^2+V_\delta^2}) \end{aligned}$$

Notice that these equations do not satisfy "charge conservation" with regard to the drain-source charge—over a bias cycle, the device can "pump" charge from the drain to the source. It can be argued that this is not a problem[1, 7]. However, it means that these equations may be difficult to implement in simulators whose capacitance is always the derivative of an internal state variable (charge). Caveat emptor...

4 Temperature Effects

An important aspect of modeling the MESFET is a correct description of the behavior as a function of temperature. Notice that V_{max} uses the temperature for V_{bi} to provide tracking.

$$I_s(T) = I_s \exp((T/T_{nom} - 1)qE_g/nkT)(T/T_{nom})^{X_{ti}/n} \quad (13)$$

$$V_{to}(T) = V_{to} + V'_{to}(T - T_{nom}) \quad (14)$$

$$V_{bi}(T) = V_{bi} + V'_{bi}(T - T_{nom}) \quad (15)$$

$$V_{max}(T) = V_{max} + V'_{bi}(T - T_{nom}) \quad (16)$$

$$\alpha(T) = \alpha \cdot 1.01^{\alpha'(T - T_{nom})} \quad (17)$$

$$\beta(T) = \beta \cdot 1.01^{\beta'(T - T_{nom})} \quad (18)$$

$$\gamma(T) = \gamma + \gamma'(T - T_{nom}) \quad (19)$$

$$R_g(T) = R_g(1 + R'_g(T - T_{nom})) \quad (20)$$

$$R_s(T) = R_s(1 + R'_s(T - T_{nom})) \quad (21)$$

$$R_d(T) = R_d(1 + R'_d(T - T_{nom})) \quad (22)$$

$$C_{gs}(T) = C_{gs}(1 + C'_{gs}(T - T_{nom})) \quad (23)$$

$$C_{gd}(T) = C_{gd}(1 + C'_{gd}(T - T_{nom})) \quad (24)$$

5 Model Parameters and Scaling

Parameter	Symbol	Description	Units	Default	Scaling
LEVEL	—	model index (-1 for TOM-2)			
VTO	V_t	Threshold voltage	volt	-2.5	—
ALPHA	α	Knee-voltage parameter	volt^{-1}	2.0	—
BETA	β	Tranconductance parameter	amp/volt^{-Q}	0.1	—
GAMMA	γ	Threshold shifting parameter	volt$^-1$	0	—
DELTA	δ	Output feedback parameter	volt	0.2	$1/w$
Q	Q	Power-law parameter	—	2	—
NG	N_g	Subthreshold slope gate parameter	—	0	—
ND	N_d	Subthreshold slope drain pull parameter	volt$^-1$	0	—
TAU	τ	Conduction current delay time	sec	0	—
RG	R_g	Gate ohmic resistance	ohm	0	—
RD	R_d	Drain ohmic resistance	ohm	0	$1/w$
RS	R_s	Source ohmic resistance	ohm	0	$1/w$
IS	I_s	Gate diode saturation current	amp	1×10^{-14}	—
N	n	Gate diode ideality factor	—	1	—
VBI	V_{bi}	Gate diode built-in potential	volt	1.0	—
VDELTA	V_δ	Capacitance transition voltage	volt	0.2	—
VMAX	V_{max}	Gate diode capacitance limiting voltage	volt	0.95	—
CGD	C_{gd}	Gate-to-drain "zero-bias" capacitance	farad	0	w
CGS	C_{gs}	Gate-to-source "zero-bias" capacitance	farad	0	w
CDS	C_{ds}	Drain-to-source capacitance	farad	0	w
EG	E_g	Barrier height	volt	1.11	—
XTI	X_{ti}	I_s temperature exponent	—	0	—
VTOTC	V'_{to}	V_{to} temperature coefficient(linear)	volt/°C	0	—
VBITC	V'_{bi}	V_{bi} temperature coefficient(linear)	volt/°C	0	—
ALPHATCE	α'	α temperature coefficient(exponential)	%/°C	0	—
BETATCE	β'	β temperature coefficient(exponential)	%/°C	0	—
GAMMATC	γ'	Linear temperature coefficient for γ	°C^{-1}	0	—
TRG1	R'_g	Linear temperature coefficient for R_g	°C^{-1}	0	—
TRD1	R'_d	Linear temperature coefficient for R_g	°C^{-1}	0	—
TRS1	R'_s	Linear temperature coefficient for R_g	°C^{-1}	0	—
CGDTCE	C'_{gdo}	Linear temperature coefficient for C_{gd}	°C^{-1}	0	—
CGSTCE	C'_{gso}	Linear temperature coefficient for C_{gso}	°C^{-1}	0	—
KF	K_f	Flicker noise coefficient		0	—
AF	A_f	Flicker noise exponent		1	—

A Expressions for the Conductances

SPICE and many SPICE-like simulators, including Pspice require analytical expressions for the conductances to be supplied. These expressions are used to compute small-signal parameters and in the Newton-Raphson integration routines. Expressions for the conductances are presented in this section. These expressions are derived directly from the expressions in section 3.1.

In addition to expressions for the current sources, Pspice requires expressions for the conductances. To facilitate the computation, it is convenient to define a current reduction factor, p. p is defined with reference to equation 1 as follows:

$$p = \frac{1}{1 + \delta V_{ds} I_{dso}} = 1 - \delta V_{ds} I_{ds} \tag{25}$$

adn express g_m and g_{ds} thus:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = g_{mo} p^2 \tag{26}$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = g_{dso} p^2 - \delta I_{ds}^2 \tag{27}$$

Differentiating equation 2 with respect to V_{gs} and V_{ds}, we obtain:

$$g_{mo} = \frac{\partial I_{dso}}{\partial V_{gs}} = \frac{I_{dso}}{V_g} \frac{Q}{\left[\exp - \left(\frac{V_{gs} - V_{to} + \gamma V_{ds}}{Q V_{st}}\right) + 1\right]} \tag{28}$$

and

$$\begin{aligned} g_{dso} &= \frac{\partial I_{dso}}{\partial V_{ds}} \qquad (29) \\ &= g_m \left(\gamma - N_d \frac{V_{gs} - V_{to} + \gamma V_{ds}}{N_g + N_d V_{ds}}\right) + \frac{Q N_d I_{dso}}{N_g + N_d V_{ds}} + \frac{\alpha \beta V_g^Q}{(1 + (\alpha V_{ds})^2)^{3/2}} \end{aligned}$$

And finally, for the gate diode:

$$g_{gs} = \frac{\partial I_{gs}}{\partial V_{gs}} = \frac{q I_s}{nkT} e^{q V_{gs}/nkT} \tag{30}$$

$$g_{gd} = \frac{\partial I_{gd}}{\partial V_{gs}} = \frac{q I_s}{nkT} e^{q(V_{gs} - V_{ds})/nkT} \tag{31}$$

B Subthreshold current

The essentials of the subthreshold model are described by Godfrey[3] where the formulas are used to describe CMOS subthreshold behavior. Godfrey dubs the model the EVO for workers that described this model in conferences, thesis and publications going back to 1983. He attributes the formula to originally Oguey[5], and traces the development by Vittoz[9], and Enz[2].

Parker and Skellern[6] used this formulation to describe subthreshold behavior in GaAs MESFETs, noting that unlike most other formulations it "provides a smooth and continuously differentiable transition between the high-current and subthreshold regions."

This equation seems to be a purely mathematical device to get a smooth transition to the subthreshold region — it doesn't have a simple physical interpretation. The behavior is thus:

$$V_g^Q(x) \approx \begin{cases} (V_{gs} - V_{to} + \gamma V_{ds})^Q, & \text{if } V_{gs} > V_{to} - \gamma V_{ds}\,; \\ (QV_{st})^Q \exp\left(\frac{V_{gs} - V_{to} + \gamma V_{ds}}{V_{st}}\right), & \text{if } V_{gs} < V_{to} - \gamma V_{ds}\,. \end{cases} \tag{32}$$

One thing to notice is the interpretation of "subthreshold slope". Usually, this is given in milli-volts per decade, and is related to N_{st} as follows if the measurement is performed at room temperature:

$$N_{st} \approx N_g \approx \ln 10 \times \frac{\text{mV/decade}}{kT/q} \approx \frac{\text{mV/decade}}{60mV} \tag{33}$$

The last part of this equation assumes that the slope is measured at room temperature. For QED devices, this works out to $N_{st} \approx 1.6$.

References

[1] Dileep Divekar. Comments on "gaas fet devices and circuit simulation in SPICE". *IEEE Trans. on Elect. Devices*, ED-34(12):2564, December 1987.

[2] C. C. Enz. *Thesis 802: High Precision CMOS Micropower Amplifiers.* PhD thesis, Ecole Polytechnique Federale de Lausanne, Aug 1989.

[3] Michael D. Godfrey. CMOS device modeling for subthreshold ciruits. *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, 39(8):532–539, Aug 1992.

[4] Angus J. McCamant, Gary D. McCormack, and David H. Smith. An improved GaAs MESFET model for SPICE. *IEEE Tran. Microwave Theory and Tech.*, 38(6):822–824, June 1990.

[5] H.J. Oguey and S. Cserveny. MOS modeling at low current density. June 1983. Presented at the Summer course on Process and Device and device Modeling, ESAT Leuven-Heverlee, Belgium.

[6] Anthony E. Parker and David J. Skellern. Improved MESFET characteristication for analog circuit design and analysis. In *IEEE GaAs IC Symposium Technical Digest*, pages 225–228, 19.

[7] I. W. Smith, H. Statz, H. A. Haus, and R. A. Pucel. On charge nonconservation in fet's. *IEEE Trans. on Elect. Devices*, ED-34(12):2565–2568, 1987.

[8] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus. GaAs FET device and circuit simulation in SPICE. *IEEE Trans. on Elect. Devices*, ED-34:160–169, 1987.

[9] E. A. Vittoz. Micropower techniques. In Y. Tsividis and P. Antognetti, editors, *Design of MOS VLSI Circuits for Telecommunications*, pages 104–144. Prentice-Hall, 1985.