## CONCLUSION

In this dissertation we developed the methods and algorithms of Logic Differential (LD) Calculus related to the problems of Computed-Aided Design of Multiple-Valued devices. Author's objective is to bring methods of LD Calculus closer to engineering practice.

New results in the applied theory of LD Calculus. Modern LD Calculus has been developed based on the generalization of Boolean Differential Calculus for MVL functions. The traditional methods and algorithms of computations of LD Calculus operators are represented by symbolic mathematical tools. The basis of our study was the matrix approach. We developed early results by applying methods of matrix algebra.

We presented LD Calculus in matrix notation for the first time.
Our approach based on matrix tools

- studied the results obtained in the area from the unified position,
- overcame the theoretical difficulties and developed the theory of LD Calculus.

It allows us to conclude that the main result of this dissertation consists in the development, systematization and generalization of the applied LD Calculus theory.

The most important theoretical results are:

- Synthesis of a class of matrix algorithms to calculate Boolean Differential operators,
- New LD operators for MVL functions introduced with respect to the criteria of reconciliation with fixed polarity RM expansions, or logic Taylor series,
- Matrix methods to solve logic equations and logic Differential equations in RM forms, and
- New LD operators introduced for arithmetical polynomial domain.

New results in the MVL Design. A particular significance for engineering practice presented in the dissertation is the generalized $D$-algorithm for MVL combinational circuits, where the generation of the $D$-cubes is maintained by LD operators.

Besides, there has been developed in the dissertation

- A technique to compute LD operators, including systolic arrays and homogeneous structures,
- A generalized method and algorithms to minimize incompletely specified MVL functions in RM and Arithmetical Polynomial domain;
- A generalized $D$-algorithm for test detection in MVL combinational circuits,
- An algorithm for sensitivity analysis of MVL network, and
- A method of circuit analysis (fault analysis, decomposition).

In general, the mentioned theoretical and applied results are important steps to incorporating LD Calculus methods into the frameworks of practical application.

Future work. The MVL design methods are connected closely with the technology to manufacture the MVL devices. This is a dynamic and flexible area both on the implementation and theoretical levels. So, the methods and algorithms that have been developed in the dissertation must be attuned to present day technology achievements and requirements. The presented matrix tools to calculate LD Operators is a good base to synthesize parallel algorithms on the homogeneous architectures of different types (systolic arrays, FPGA and other parallel structures).

The techniques such as BDD which are intensively developed in Logic Design and are applied for RM domain synthesis, also have all premises to be used in the area. This problem was considered in part here to calculate LD operators for MVL functions. Further steps are required to develop the BDD techniques to solve the applied problems solved by LD Calculus methods.

The forming of the theory of LD Calculus is not complete without investigations and generalizations in the arithmetical polynomial domain. These operators require further development to be harmoniously integrated into the area.

The circle of the applied problems solved by LD Calculus methods have to be extended taking into account recent achievements of the MVL Design. The present dissertation does not concern the graph analysis problem, design of sequential circuits, applications in the automata theory and others. Being developed from the Boolean Differential Calculus, LD Calculus theory has not found such wide application as the Boolean one. It can be said that the main operators of LD Calculus and its application to solve several important problems of MVL design are the basis to investigate and develop this direction.

## REFERENCES

Abd-El-Bar M.H., and Vranesic Z.G. (1989), Charge-Coupled Device Implementation of Multivalued Logic System, IEE Proc., vol. 136, Pt.E, no. 4, pp. 306-315
Agrawal V. (1981), An Information Theoretic Approach to Digital Fault Testing, IEEE Trans. Computers, vol. C-30, no. 8, pp. 582-587
Agrawal V., Pugsley J.H., and Silio C.B. (1984), Multiple Valued Output ROM Circuits, Proc. $14^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 224-231
Ahmed N., and Rao K.R. (1975), Orthogonal Transforms for Digital Signal Processing, SpringerVerlag, Berlin
Akers S.B. (1959), On a Theory of Boolean Functions, J. of Soc. Ind. Appl. Math., 7, pp. 487-498
Akers S.B. (1976), A Logic System for Fault Test Generation, IEEE Trans. Computers, vol. C-25, pp. 620-629
Akers S.B. (1978), Binary Decision Diagrams, IEEE Trans. Computers, vol. C-27, no. 6, pp. 509-516
Allen C.M., and Givone D.D. (1977), The Allen-Givone Implementation Oriented Algedra, In book: Computer Science and Multiple-Valued Logic, Rine D.C. (Ed.), North Holland, Amsterdam, Chap. 9
Amar V., and Condulmari N. (1967), Diagnosis of Large Combinational Networks, IEEE Trans. Electron. Comput, vol. EC-16, pp. 675-680
Antonenko V., Guvakov I., Shmerko V., Kaczmarek A., and Yanushkevich S. (1995), Linear Arithmetical Forms of $k$-Valued Functions, Proc. European Conf. on Circuit Theory and Design, Turkey, pp. 323-328
Aoki T., Kameyama M., and Higuchi T. (1991), Design of Interconnection-Free Biomolecular Computing System, Proc. 21th IEEE Symp. on Multiple-Valued Logic, pp. 173-180
Armstrong D.B. (1966), On Finding a Nearly Minimal Set of Fault Detection Tests for Combinational Logic Nets, IEEE Trans.on Electronic Computers, vol. EC-15, no. 1, Feb., pp. 66-73
Artukhov V., Kondratiev V., and Shalyto A. (1982), Generating Boolean Functions via Linear Arithmetic Polynomials, Automation and Remote Control (USA), vol. 43, no. 4, Part 1, pp. 505515
Bartlett K., Brayton R., Hachtel G., Jacoby R., Morrison C., Rudell R., Sangiovanni-Vincentelli A., and Wang A. (1988), Multi-Level Logic Minimization Using Implicit Don't Cares, IEEE Trans. on Computer-Aided Design, vol. 7, no. 6, pp. 723-740
Bell N., Page E.W., and Thomason M.G. (1972), Extension of the Boolean Difference Concept to Multivalued Logic Systems, Proc. Int. Symp. Theory and Applications of Multiple-Valued Logic Design, pp. 17-24
Bennets R.(1982), Analysis of Reliability Block Diagrams by Boolean Techniques, IEEE Trans. on Reliab., vol. 31, pp. 156-166
Benten M.S.T., and Sait S.M. (1994), GAP: A Genetic Algorithm Approach to Optimize Two-Bit Decoder PLAs, Int. J. of Electronics, vol. 76, no. 1, pp. 99-106
Bernstein B.A. (1924), Operations with Respect to which the Elements of a Boolean Algebra Form a Group, Trans. Amer. Math. Soc., vol. 26, pp. 171-175
Besslich Ph.W. (1983), Efficient Computer Method for EXOR Logic Design, IEE Proc., vol. 130, Pt.E, no. 6, pp. 203-206
Bochmann D., and Posthoff Ch. (1981), Binare Dinamische Systeme, Springer-Verlag, Berlin
Bochmann D., and Steinbach B. (1991a), Logikentwurf mit XBOOLE, Verlag Technik, Berlin

Bochmann D., Dresig F. and Steinbach B. (1991b), A New Decomposition Method for Multilevel Circuit Design, Proc. EDAC-91, Amsterdam, pp. 374-377
Bochmann D. (1997), Modelle fur Ereignisdiskrete Systeme im Booleschen Differentialkalkul, Automatisierungstechnic, 1997, no. 3. pp. 99-106
Bochmann D., Stankovic R., Tosic Z., Shmerko V., and Yanushkevich S. (1998), Logic Differential and Integral Calculus: History, Achivements, and Trends, will be published in Automation and Remote Control (USA)
Bondar I., Kaczmarek A., Yanushkevich S., and Shmerko V. (1995), State of the Art to use Discrete Orthogonal Transforms for Canonical Expansions of Boolean Functions, Proc. Int. Conf. on Computer-Aided Design of Discrete Devices - CAD DD'95, Minsk, Belarus, pp. 43-52
Boole G. (1847), The Mathematical Analysis of Logic, Being an Essay Towards a Calculus of Deductive Reasoning, Macmillan, Cambridge; George Bell, London, Reprints 1948, 1951, Basil Blackwell, Oxford
Brand D., and Sasao T. (1993), Minimization of AND-EXOR Expressions Using Rewrite Rules, IEEE Trans. Computers. vol. 42, no 5, pp. 568-576
Brayton R.K., McMullen T., Hachtel G.D., and Sangiovanni-Vincentelli A.L. (1984), Logic Minimization Algorithms for VLSI Synthesis, Kluwer Academic Publishers
Bryant R.E. (1986), Graph-Based Algorithms for Boolean Function Manipulation, IEEE Trans. Computers, vol. C-35, no. 8, pp. 667-691
Brayton R.K, McGeer P., Sanghavi J.V., and Sangiovanni-Vincentelli A.L. (1993), A New Exact Minimizer for two-Level Logic Synthesis, pp. 1-31, In Book: Logic Synthesis and Optimization T. Sasao (Ed.) Kluwer Academic Publishers

Brown F.M. (1970), Reduced Solution of Boolean Equations, IEEE Trans. Computers, vol. C-19, pp. 976-981
Brusentzov N.P. et.al. (1962), The SETUN Small Automatic Digital Computer, Vest. Moscow Univ., no. 4, pp. 3-12 (In Russian)
Butzer P.L., and Stankovic R.S., (Eds.) (1990), Theory and Applications of Gibbs Derivatives, Matematicki Institut, Belgrade, Yugoslavia
Capasso F., Sen S., etc. (1989), Quantum Functional Devices: Resonant-Tunneling Transistors, Circuits with Reduced Complexity and Multiple-Valued Logic, IEEE Trans. Electron Devices, vol. 36, no. 10., pp. 2065-2082
Chang C.C., and Falkowski B.J. (1995), Flexible Optimization of Fixed Polarity Reed-Muller Expansions for Multiple output Completely and Incompletely Specified Boolean Functions, Proc. Asia and South Pacific Design Automation Conf., Chiba, Japan, pp. 335-340
Chang Y.Y., and Butler J.T. (1991), The Design of Current Mode CMOS Multiple-Valued Circuits, Proc. $21^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 130-138
Chang Y.-J., Lee C.L. and Chen J.E. (1996), Fault Models for the Multi-Valued Current Mode CMOS Circuits, unpublished paper, presented at $26^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic
Cheushev V., Shmerko V., D.Simovici D., Yanushkevich S. (1998), Information estimations for logical functions, Proc. IEEE $28^{\text {th }}$ Int. Symp. on Multiple-Valued Logic, Japan
Chiang K.W., and Vranesic Z.G. (1982), Fault Detection in Ternary nMOS and CMOS Circuits, Proc. $12^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 129-138
Chi-Hong Hwang, and A.C.- H.Wu (1997), An Entropy Measure for Power Estimation of Boolean Functions, Proc. of the ASP-DAC'97 - Asia and South Pacific Design Automation Conference, Japan, pp. 101-106
Cho Y.H., and Mouftan H.T. (1988), A CMOS Ternary ROM Chip, Proc. $18^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 358-363
Clarke E.M., Fujita M., and Zhao X. (1996), Multi-Terminal Binary Decision Diagrams and Hybrid Decision Diagrams, In Book: T. Representations of Discrete Functions, T. Sasao (Ed.), Kluwer Academic Publishers, pp. 93-108

Coy W., and Moraga C. (1979), Description and Detection of Faults in Multiple-Valued Logic Circuits, Proc. $19^{\text {th }}$ IEEE Int. Symp. on Muliple-Valued Logic, pp. 74-81
Csanky, L., Perkowski M., and Schaefer I. (1993), Canonical Restricted Mixed-Polarity Exclusive-OR Sums of Products and the Efficient Algorithm for their Minimisation, Proc. IEE, Pt. E, vol. 140, no. 1, pp. 69-77
Current K.W. (1993) Multiple Valued Logic: Current-mode CMOS Circuits, Proc. $23^{\text {rd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 176-181
Damarla T., and Karpovski M. (1989), Fault - Detection in Combinational Networks by Reed-Muller Transforms, IEEE Trans. Computers, vol. C-38, no. 6, pp. 788-797
Damarla T. (1992), Generalized Transforms for Multiple-Valued Logic Circuits and their Fault Detection, IEEE Trans. Computers, vol. C-41, no. 9, pp. 1101-1109
Davio M., Thayse A., and Bioul G. (1972), Symbolic Computation of Fourier Transform of Boolean Functions, Philips Res. Rep, no. 27, pp. 386-403
Davio M. (1973), Taylor Expansion of Symmetric Boolean Functions, Philips Res. Repts., vol. 28, pp. 466-474
Davio M., Deschamps P., and Thayse A. (1978), Discrete and Switching Functions, Georgi Publishing Co. and N.J.- McGraw-Hill, Inc.
Davio M., and Deschamps J.-P. (1981), Synthesis of Discrete Functions Using I²L Technology, IEEE Trans. Computers, vol. C-30, pp. 653-661
Debany, W.H.Jr., Hartmann C.R.P., and Snethen T.J. (1991), Algorithm for Generating Optimal Tests for Exlusive-OR Networks. IEE Proc.E, vol. 138, no. 2, pp. 93-96
Debnath D., and Sasao T. (1996), GRMIN2: A Heuristic Simplification Algorithm for Generalized Reed-Muller Expressions, IEE Proceedings on Computing and Digital Techniques, vol. 143, no. 6, pp. 376-384
DeMicheli G. (1994), Synthesis and Optimization of Digital Circuits. New York: McGraw Hill
Deng X., Hanyu T., and Kameyama M. (1994), Design and Evaluation of a Current-Mode MultipleValued PLA based on a Resonant Tunnelling Transistor Model, IEE Proc. Circuit Devices Syst., vol. 141, no. 6, pp. 445-450
Deng X., Hanyu T., and Kameyama M. (1995), Quantum-Device-Oriented Multiple-Valued Logic System Based on a Pass Gate, IEICE Trans. Information and Systems, vol. E78-D, no. 8, pp. 951-958
Dill R.M., and Perkowski M. (1998), Evolutionary Minimization of Generalized Reed-Muller Forms, Proc. Int. Conf. on Computational Inelligence and Multimedia Applications, H.Servaraj, and B.Verma (Eds), Australia, pp. 727-733

Donohue B., Holly P., and Ilgenstein K. (1985), A 256-k HCMOS ROM Using Four State Cell Approach, IEEE J. Solid-State Circuits, vol. C-20, pp. 256-262
Drechsler R., Sarabi A., Theobald M., Becker B., and Perkowski M. (1994), Efficient Representation and Manipulation of Switching Functions Based on Ordered Kronecker Functional Decision Diagrams, Proc. Design Automation Conf., pp. 415-419
Drechsler R., Hengster H., Schaefer H., and Becker B. (1996), Testability of AND-EXOR Expressions, Proc. IEEE European Test Workshop, Montpellier
Dueck G.W., Earle R.C., Tirumalai P., and Butler J.T. (1992), Multiple-Valued Programmable Logic Array Minimization by Simulated Annealing, Proc. $22^{\text {nd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 66-74
Edwards C.R. (1978), The Gibbs Dyadic Differentiator and its Relationship to the Boolean Difference, Computers and Electronic Engineering, vol. 5, no 4, pp. 335-344
Etiemble D., and Israel M. (1974), A New Concept for Ternary Logic Elements, Proc. $4^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 437-458
Etiemble D., Chanussot C., and Nevi V. (1990), 4-Valued BiCMOS Circuits for the Transmission System of a Massively Paralleling Architecture, Proc. $20^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 348-354

Falkowski B., and Perkowski, M. (1990), A Family of All Essential Radix-2 Addition/Subtraction Multi-Polarity Transforms: Algorithms and Interpretations in Boolean Domain, Proc. $23^{\text {rd }}$ IEEE Int. Symp. on Circuits \& Systems, New Orleans, USA, pp. 2913-2916
Falkowski B., and Chang C.H. (1994), Efficient Algorithms for the Calculation of Arithmetic Spectrum from OBDD and Synthesis of OBDD from Arithmetic Spectrum for Incompletely Specified Boolean Functions, Proc. $27^{\text {th }}$ IEEE Int. Symposium on Circuits and Systems, London, UK, vol. 1, pp. 197-200
Falkowski B., and Chang C.H. (1995a), Generation of Multi-Polarity Arithmetic Transform from Reduced Representation of Boolean Functions, Proc. $28^{\text {th }}$ IEEE Int. Symp. on Circuits and Systems, pp. 2168-2171
Falkowski B., and Rahardja S. (1995b), Quasi-Arithmetic Polynomial Expansions for Quaternary Functions, Proc. IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Japan, pp. 265-272
Falkowski B., Shmerko V., and Yanushkevich S. (1997a), Arithmetic Logic - Its Status and Achivements, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 208223
Falkowski B.J., Holowinski G., Malecki K. (1997b), Effective Minimization of Logic Functions in Reed-Muller Domain, Proc. Int. Conf. on Applications of Computer Systems, Poland, pp. 248-255
Fejer P., and Simovici D. (1991), Mathematical Foundations of Computer Science, vol. 1, Springer Verlag
Fogarty T.C., Miller J.F., and Thomson P. (1998), Evolving Digital Logic Circuits on Xilinx 6000 Family FPGAs. In book: Soft Computing in Engineering Design and Manufacturing, P.K.Chawdry, R.Roy, and R.K.Pant (Eds), Springer-Verlag, London, pp. 299-305

Franke D. (1992), A Novell Approach to Finite Automata with Control Application for Transport Systems, Proc. IEE Int. Conf. on Intelligent Systems Engineering, Edinburgh, UK, no. 36, pp. 7176
Franke D. (1995), Arithmetic Modelling - a Link Between Discrete-Time Systems and Binary Process Control, Appl. Math. and Comp. Sci., vol. 5, no. 3, pp. 511-521
Fujiwara H., and Shimono T. (1983), On the Acceleration of Test Generation Algorithms, IEEE Trans. Computers, vol. TC-32, pp. 1137-1144
Fujiwara H. (1985), Logic Testing and Design for Testability, MIT Press, Cambridge, Massachusetts
Gavrilov M.A., and Zakrevskij A.D. (Eds.) (1969), LYaPAS: A Programming Language for Logic and Coding Algorithms, Academic Press, N.Y.
Gibbs J.E. (1969), Walsh Functions as Solutions of a Logical Differential Equations, National Physical Lab., Teddington, UK, DES Report, no. 1
Goel P. (1981), An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits, IEEE Trans. Computers, vol. C-30, pp. 215-222
Green D.H. (1986), Modern Logic Design, Academic Press
Green D.H. (1987), Reed-Muller Expansions of Incompletely Specified Functions, Proc. IEE, Pt. E, 134, pp. 228-236
Green D.H. (1989), Ternary Reed-Muller Switching Functions with Fixed and Mixed Polarity, Int. J. Electronics, 67, pp. 761-775
Green D.H. (1991), Families of Reed-Muller Canonical Forms, Int. J. Electronics, vol. 70, no. 2, pp. 259-280
Guima T.A., and Katbab A. (1988), Multivalued Logic Integral Calculus, Int. J. Electronics, vol. 65, pp. 1051-1066
Guima T.A., and Tapia M.A. (1987), Differential Calculus for Fault Detection in Multivalued Logic Networks, Proc. $17^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 99-108
Hammer P.L, and Rudeanu S. (1968), Boolean Methods in Operational Research and Related Areas, Springer, Berlin

Hanyu T., and Higuchi T. (1989), High-Density Quaternary Logic Array Chip for Knowledge Information Processing Systems, IEEE J. Solid-State Circuits, vol. SC-24, no. 4, pp. 916-921
Hanyu T., Arakaki M. and Kameyama M. (1997), One-Transistor-Cell 4-valued Universal-Literal CAM for Cellular Logic Image Processing, Proc. $27^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 175-180
Hao-Yung Lot, and Chien-Chun Su (1989), A Distributive D-Algorithm for Generating the Test Pattern for Faulty Combinational Circuit, Int. J. Electronics, vol. 66, no. 1, pp. 35-42
Harking B. (1990), Efficient Algorithm for Canonical Reed-Muller Expansions of Boolean Functions, IEE Proc.E, Computers and Digital Techniques, vol. 137, pp. 366-370
Hartman F. (1967), Boolean Differential Calculus, IBM Internal Report, TR22.526
Hartmann C.R.P., Varshney P.K., Mehrotra K.G., and Gerberich C.L. (1982), Application of Information Theory to the Construction of Efficient Decision Trees, IEEE Trans. Inf. Theory., vol. IT-28, pp. 565-577
Heidtmann, K.D. (1991), Arithmetic Spectrum Applied to Fault Detection for Combinational Networks, IEEE Trans. on Comp., vol. 40, no. 3, pp. 320-324
Holowinski G., and Yanushkevich S. (1996), Fast Heuristic Minimization of MVL Functions in Generalized Reed-Muller Domain, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 57-64
Holowinski G. (1997), Parallel Version of Generalized Zakrevskij's Algorithm for Minimization of Weakly Specified Multi-Valued Functions, Proc. Int. Conf. on Pattern Recognition \& Information Processing, Minsk, Belarus, vol. 1, pp. 332-339
Hong S.J., Cain R.G., and Ostapko D.L. (1974), MINI: A Heuristic Approach for logic Minimization, IBM J. Res. Develop., 18 (5), , pp. 443-458
Hunt S. (1975), Artificial Intelligence, Addison-Wesley
Hurst S.L. (1978), Logic Processing of Digital Signals, Grawe Russak \& Edward Adward Arnold
Hurst S.L. (1984), Multiple-Valued Logic - Its Status and Its Future, IEEE Trans. Computers, vol. C33, no. 12, pp. 1160-1179
Hurst S.L., Miller D.M., and Muzio J.C. (1985), Spectral Techniques in Digital Logic, Academic Press, N.J.
Iba H., Iwata M., and Higuchi T. (1996), Machine Learning Approach to Gate-Level Evolvable Hardware, Lecture Notes in Computer Science, no. 1259, T.Higuchi, M.Iwata, and W.Liu (Eds), Springer-Verlag, pp. 327-393
Iravani K., and Perkowski M. (1998), Image Compression Based on Reed-Muller Transforms, Proc. Int. Conf. on Computational Inelligence and Multimedia Applications, H.Servaraj, and B.Verma (Eds), Australia, pp. 727-733
Ishizuka O. (1977), On Multivalued Multithreshold Networks Composed of Conventional Threshold Elements, IEEE Trans. Computers, vol. C-26, no. 12, pp. 1251-1257
Ishizuka O., Takarabe H., etc. (1991), Synthesis of Current-Mode Pass Transistor Networks, Proc. $21^{\text {st }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 139-146
Ivanescu P.L., and Rudeanu S. (1966), Pseudo-Boolean Methods for Bivalent Programming, Lecture Notes Math., 23, pp. 1114-1122
Jain A.K., Abd-El-Barr M.H., and Bolton R.J. (1993a), A New Structure for CMOS Realization of MVL Functions . Int. J. Electronics, vol. 74, no. 2, pp. 256-263
Jain A.K., Bolton R.J., and Abd-El-Barr M.H. (1993b), CMOS Multiple-Valued Logic Design. Part I: Circuit Implementation. Part II: Function Realization, IEEE Trans. Circuits and Systems, vol. 40, no. 8, pp. 503-522
Jain J.(1996), Arithmetic Transform of Boolean Functions. In book: Representations of Discrete Functions T. Sasao and M.Fujita (Eds.), Kluver Academic Publishers, pp. 133-161
Jaroszewicz S., Shmerko V., and Yanushkevich S. (1996), Exact Irredundant Searching for a Minimal Reed-Muller Expansion for an Incompletely Specified MVL Function, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 65-74

Józwiak L., and Konieczny P. (1996), Input Support Minimization for Efficient PLD and FPGA Synthesis. Proc Int. Workshop on Logic and Architecture Synthesis, Grenoble, pp. 30-32
Kabakcioglu A.M., Varshney P.K., and Hartman C.R.P. (1990), Application of Information Theory to Switching Function Minimization, IEE Proc., Pt E, vol. 137, pp. 389-393
Kaczmarek A., Levashenko V., Majka E., and Yanushkevich S. (1994a), Method to Solve Boolean Differential Equations on Systolic Arrays, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 39-48
Kaczmarek A., Majka E., and Yanushkevich S. (1994b), Tree-network Systolic Architecture for Computing Test Vectors of Combinational Circuits, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 55-58
Kaczmarek A., Shmerko V., Yanushkevich S., and Wojciechowski D. (1995), Neural Networks for Logic Control Based Arithmetical Logic, Proc. Int. Symp. on Methods and Models in Automation \& Robotics, Miedzyzdroje, Poland, pp. 769-774
Kalganova T., Kochergov E., Zaitseva E., and Yanushkevich S. (1996), A Genetic Approach to Optimise Polynomial Forms of Incompletely Specified MVL Functions, Proc. Workshop on Evolutionary Computing, Brighton, UK, pp. 89-102
Kalganova T., Miller J.F. (1997), Evolutionary Approach to Design Multiple-Valued Combinational Circuits, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 333-339
Kameyama M., Hanyu T., and Higuchi T. (1987), Design and Implementation of Quaternary NMOS Integrated Circuits for Pipelined Image Processing, IEEE J. Solid-State Circuits, vol. SC-22, no. 1, pp. 20-27
Kameyama M., Kawahito S., and Higuchi T. (1988a), A Multiplier Chip and Multiple-Valued Bidirectional Current-Mode Logic Circuits, IEEE Trans. Computers, vol. 21. pp. 43-56.
Kameyama M., Sekibe T., and Higuchi T. (1988b), Design of Highly Parallel Residue Arithmetic Circuits Based on Multiple-Valued Bi-Directional Current-Mode MOS Technology, Proc. $18^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 6-13
Karpovsky M.G. (Ed.) (1985), Spectral Techniques and Fault Detection, Academic Press, N.Y.
Katbab A., and Guima T. (1989), On Multivalued Logic Design Using Exact Integral Calculus, Int. J. Electronics, vol. 66, no. 1, pp. 1-18
Kawahito S., Kameyama M., and Higuchi T. (1986), VLSI-Oriented Bi-Directional Current-Mode Arithmetic Circuits Based on the Radix-4 Signed Digit Number System, Proc. $16^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 70-77
Kawahito S., Ishida M., Nakamura T., and Kameyama M. (1994), High-Speed Area-Efficient Multiplier Design Using Multiple-Valued Current-Mode Circuits, IEEE Trans. Computers, vol. C-28, no. 1, pp. 34-41
Kerkhoff H.G., and Butler J.T. (1986), Design of a High-Radix Programmable Logic Array Using Profiled Peristaltic Charde-Coupled Devices, Proc. $16^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 128-136
Kodandapani K., and Setlur R. (1975), Reed-Muller Canonical Forms to Multi-Valued Logic, IEEE Trans. Comput., vol. C-24, pp.628-636
Kopec M. (1994), An Information Theoretic Measure of Compaction Efficiency, Archives of Control Sciences (Poland), vol. 3 (XXXIX), no. 3-4, pp. 271-287
Kukharev G., Shmerko V., and Yanushkevich S. (1991), Technique of Binary Data Parallel Processing on VLSI, Vysheyshaya Shkola Publishers, Minsk, Belarus, 227 p. (In Russian)
Kumar, S.K., and Breuer, M.A. (1981), Probabilistic Aspects of Boolean Switching Functions via a New Transform, J. of ACM, vol. 28, pp. 502-520
Kung H.T., and Leiserson C.E. (1978), Systolic Arrays (for VLSI), In.book: Sparse Matrix Proceedings, SIAM, Philadelphia, pp. 256-282
Kuzmitsky V., Shmerko V., and Yanushkevich S. (1990), Binary Image Processing Algorithms on Homogeneous Computing Environment. In book: Using Computers for Signal Processing, Technical University, Riga, Latvia, pp. 5-14 (In Russian)

Labunets V.G., and Sitnikov O.P. (1975), Harmonic Analysis of Boolean and $k$-Valued Functions Over Finite Fields, The USSR Academy of Sciences Transactions, Seria "Technical Cybernetics", no. 1, pp. 141-148 (In Russian)
Lanchares J., Hidalgo J.I., and Sanchez J.M. (1997), Boolean Networks Decomposition Using Genetic Algorithms, Microelectronics J., vol. 28, pp. 551-560
Larrabee T. (1992), Test Pattern Generation Using Boolean Satisfability, IEEE Trans. ComputerAided Design, vol. 11, no. 1, pp. 4-15
Lee S.C. (1978), Modern Switching Theory and Digital Design, Prentice-Hall, N.J., pp. 48-72
Lei K., and Vranesic Z. (1991), On the Synthesis of 4-Valued Current Mode Circuits, Proc. $21^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 147-155
Levashenko V.G., Yanushkevich S.N., and Zaitseva E.N. (1995), Synthesis of Parallel Algorithms to Compute Derivatives of MVL-Functions, Proc. Workshop on Sampling Theory \& Applications, Riga, Latvia, pp. 319-322
Levashenko V., Shmerko V., and Yanushkevich S. (1996a), Solution of Boolean Differential Equations on Systolic Arrays, Cybernetics and System Analysis (USA), vol. 32, no. 1, pp. 26-40
Levashenko V., Yanushkevich S., and Majka E. (1996b), Hardware Support to Detect Test For MValued Switching Circuits Based on Roth's Algorithm Generalization, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 83-96
Liang-Chia, Chen, and Twu Hong-Tay (1995), Synthesis of Multilevel NAND Gate Circuits For Incompletely Specified Multi-Output Boolean Functions and CAD Using Permissible Cubes and PCRM Graphs, Int. J. Electronics, vol. 78, no. 2, pp. 303-316
Ligmanowski M. (1969), A Method for Solving a System of Logical Equations, Arch. Automat. i Telemech. vol. 14, pp. 131-143 (In Polish)
Lloris-Ruiz A., Gomez-Lopera J.F., and Roman-Roldan R. (1993), Entropic Minimization of MultipleValued Functions, Proc. $23^{\text {rd }}$ Int. Symp. on Multiple-Valued Logic, pp. 24-28
Lo H.Y. (1980), Generalized Fault Detection for Multivalued Logic Systems, Proc. $10^{\text {th }}$ IEEE Int. Symp. on Muliple-Valued Logic, pp. 178-186
Lo.H.Y., and Lee S.H. (1981), A Map-Partition Method for the Fault Detection of Multi-Valued and Multi-Level Combinational Logic Circuits, Proc. $11^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 283-289
Lu H., and Lee S.C. (1984), Fault Detection in M-Logic Circuits Using the M-Difference, Proc. 14th Int. Symp. on Multiple-Valued Logic, pp. 62-70
Lu H., and Lee S.C. (1985), M-Algebra, Proc. $15^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 272-284
Łuba T., Lasocki R., and Rybnik J. (1993a), An Implementation of Decomposition Algorithm and its Application in Information Systems Analysis and logic Synthesis, Proc. Int. Workshop on Rough Set and Knowledge Discovery - RSKD'93, Canada, pp. 487-498
Łuba T., and Rybnik J. (1993b), Algorithmic Approach to Discernibility Function with respect to Attributes and Objects Reduction, Foundation of Computing and Decision Sciences, vol. 18, no. 3-4, pp. 241-258
Łuba T., and Selvaraj H. (1995a) A General Approach to Boolean Functions Decomposition and its Application in FPGA-Based Synthesis, VLSI Design, vol. 3, no. 3-4, pp. 289-300
Łuba T. (1995b), Decomposition of Multiple-Valued Functions, Proc. $25^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 256-263
Łuba T., Jasiński K., Zbierzchowski B. (1997), Specjalizowane Uklady Cyfrowe w Strukturach PLD i FPGA, Wydawnictwa Komunikacji i Łaczności, Warszawa (In Polish)
Lukasiewicz J. (1920), 3-valued Logic, Ruch Filozoficzny, no. 5, pp. 169-171 (In Polish)
Malyugin V. (1982), Representation of Boolean Functions by Arithmetical Polynomials, Automation and Remote Control (USA), vol. 43, no. 4, Part 1, pp. 496-504
Malyugin V. (1984), Realization of Boolean Function's Corteges by Means of Linear Arithmetical Polynomials, Automation and Remote Control (USA), vol. 45, no. 2, Part 1, pp. 239-245

Malyugin V. (1987), Arithmetical Representation of Petri Nets, Automatics and Telemechanics, USSR Academy of Sciences, no. 5, pp. 156-164 (In Russian), Translated Automation and Remote Control (USA), vol. 48, no. 5
Marczewski E. (1948), Concerning Symmetric Difference of Sets in the Theory and in Boolean Algebra, Colloq. Math. no. 1, pp. 199-202
Margin T.L., and Current K.W. (1986), Characteristics of Prototype CMOS Quaternary Logic Encoder-Decoder Circuits, IEEE Trans. Computers, vol. C-35, no. 2, pp. 157-161
Marinos P. (1981), Derivation of Minimal Complete Sets of Test-Input Sequences Using Boolean Differences. IEEE Trans. Computers, vol. C-20, no. 1, pp. 25-32
McCluskey E.J. (1979), Logic Design of Multivalued $\mathrm{I}^{2}$ L Logic Circuits, IEEE Trans. Computers, vol. C-28, no. 8, pp. 564-559
McCluskey E.J. (1980), Logic Design of MOS Ternary Logic, Proc.10 th IEEE Int. Symp. on MultipleValued Logic, pp. 1-5
McKenzie L., Almaini A., Miller J.F., and Thomson P. (1993) Optimization of Reed-Muller Logic Functions, Int. J. Electronics, vol. 75, no. 3, 1993, pp 451-466
Michalewicz Z. (1992), Genetic Algoriths +Data Structure = Evolutionary Programs, Springer-Verlag, Berlin
Miller D.M. (1982), Spectral Signature Testing for Multiple-Valued Combinational Networks, Proc. $12^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 152-158
Miller D.M. (1993), Multiple-Valued Logic Design Tools, Proc. $23^{\text {rd }}$ IEEE Int. Symp. on MultipleValued Logic, pp. 2-11
Miller D.M. (1994), Spectral Transformation of Multiple-Valued Decision Diagrams, Proc. $24^{\text {th }}$ IEEE Symp. on Multiple-Valued Logic, pp. 89-96
Miller J.F., and Thomson, P. (1994a), Highly Efficient Exhaustive Search Algorithm for Optimizing Canonical Reed-Muller Expansions of Boolean Functions, Int. J. Electronics, vol. 76, pp. 37-56
Miller J.F., Luchian H., Bradbeer P.G., and Barclay P.J. (1994b), Using a Genetic Algorithm for Optimizing Fixed Polarity Reed-Muller Expansions of Boolean Functions, Int. J. Electronics, vol. 76, no. 4, pp. 601-609
Miller J.F., and Thomson P. (1995), Minimisation of Reed-Muller Expansions of Boolean Functions using Modern Optimisation Methods, Proc.Int. Conf. on Computer-Aided Design of Discrete Devices, Minsk, Belarus, pp. 59-68
Miller J.F., Thomson P., and Fogarty T. (1998), Designing Electronic Circuits Using Evolutionary Algorithms. Arithmetic Circuits: A case Study, In book: Genetic Algorithms and Evolution Strategies in Engineering and Computer Science, D.Guagrigella, J.Periaux, C.Poloni, G.Winter (Eds.), John Wiley \& Sons, pp. 105-131
Minsky, M., and Papert, S. (1969), Perceptrons: an Information to Computational Geometry, Cambridge, MA, MIT Press
Moraga C. (1978), Complex Spectral Logic, Proc. $8^{\text {th }}$ IEEE Int. Symp. on Multiple Valued Logic, pp. 149-156
Moraga C. (1984), Systolic Systems and Multiple-Valued Logic, Proc. $14^{\text {th }}$ IEEE Int. Symp on Multiple-Valued Logic, pp. 98-108
Moraga C. (1994), Spectral Techniques and Soft Computing, Proc. $5^{\text {th }}$ Int. Workshop on Spectral Techniques, C. Moraga, etc. (Eds.) China, pp. 1-7
Morozov A.M. (1978), Differentiation and Integration of Logic Functions, Cybernetics, Ukrainian Academy of Scinces, no. 6, pp. 33-39 (In Russian), Translated Cybernetics and System Analysis (USA)
Morozov A. (1987), Orthogonal Transforms of Logic Functions, Cybernetics, Ukrainian Academy of Scinces, no. 3, pp. 45-53 (In Russian), Translated Cybernetics and System Analysis (USA)
Mou Hu, and Dueck G. (1997), A Multiple-Valued Super Switch Algebra with Applications to Design of Quantum Device Based System, Proc. Int. Conf. on Applications of Computer Systems, Poland, pp. 256-265

Mouftan H.T., and Jordan B. (1977), Design of Ternary COSMOS Memory and Sequential Circuits, IEEE Trans. Computers, vol. C-26, pp. 281-288
Muroga S. (1979), Logic Design and Switching Theory, Wiley, New York
Muzio J.C., and Wesselkamper T.S. (1986), Multiple-Valued Switching Theory, Adam Higler Ltd. Bristol and Boston
Muzio J.C. (1988), Stuck Fault Sensitivity of Reed-Muller and Arithmetic Coefficients, Proc. $3^{\text {rd }}$ Int. Workshop on Theory and Applications of Spectral Techniques, pp. 36-45
Nagata Y., and Afuso C. (1993), A Method of Test Pattern Generation for Multiple-Valued PLA's, Proc. $23^{\text {rd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 87-91
Orlowska E. (1997), Many-Valuedness and Uncertainty, Proc. $27^{\text {th }}$ IEEE Int. Symp. on MultipleValued Logic, pp. 153-162
Parker K.P., and McCluskey, E.J. (1975a), Analysis of Logic Circuits with Faults Using Input Signal Probabilities, IEEE Trans. on Computers., vol. 24, no. 5, pp. 573-578.
Parker K.P., and McCluskey, E.J. (1975b), Probabilistic Treatment of General Combinational Networks, IEEE Trans. on Computers., vol. 24, no. 6, pp. 668-670.
Pelayo F., Garcia C., Prieto A., and Lloris A. (1989), Some Improvement in the Implementation of Multithreshold and Multivalued I ${ }^{2}$ L Circuits, Int.J. Electronics, vol. 66, no. 1, pp. 19-34
Pelayo F.J., Prieto A., etc. (1991), CMOS Current-Mode Multivalued PLA's, IEEE Trans. Circuits and Systems, vol. 38, pp. 434-441
Perkowski M., Helliwell M., and Wu P.(1989), Minimization of Multiple-Valued Input-Output MixedRadix Exclusive Sum of Products for Incompletely Specified Boolean Functions, Proc. $19^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 256-263
Perkowski, M., and Chrzanowska-Jeske, M. (1990), An Exact Algorithm to Minimize Mixed-radix Exclusive Sums of Produsts for Incompletely Specified Boolean Functions, Proc. Int. Symp. on Circuits and Systems, New Orlean, USA, pp. 1652-1655
Perkowski M. (1995a), A New Representation of Strongly Unspecified Switching Functions and its Application to Multiple-Level AND/OR/EXOR Synthesis, Proc. IFIP WG 10.5 Int. Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Japan, pp. 143-151
Perkowski M., Ross T., Gadd D., Goldman J., and Song N. (1995b), Application of ESOP Minimization in Machine Learning and Knowledge Discovery, Proc. IFIP WG 10.5 Int. Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Japan, pp. 102109
Perkowski M., Sarabi A., and Beyl F. (1995c), Fundamental Theorems and Families of Forms for Binary and Multiple-Valued Linearly Independent Logic, Proc. IFIP WG 10.5 Int. Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Japan, pp. 288-299
Perkowski M., Jozwiak L., and Drechsler R. (1997a) A Canonical AND/EXOR Form that includes both the Generalized Reed-Muller Forms and Kronecker Forms, Proc. IFIP WG 10.5 Int. Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Japan, pp. 219239
Perkowski M., Jozwiak L., and Drechsler R. (1997b), New Hierarchies of Generalized Kronecker Trees, Forms, Decision Diagrams, and Regular Layouts, Proc. IFIP WG 10.5 Int. Workshop on Applications of the Reed-Muller Expansions in Circuit Design, pp. 115-132
Pospelov D. (1974), Logical Methods for Circuit Analysis and Synthesis, Publishing House "Energia", Moscow (In Russian)
Post E.L. (1921) Introduction to a General Theory of Elementary Propositions, Amer. J. Math., vol. 43, pp. 163-185
Posthoff C. (1996), Optimal Decision Diagrams, Proc. Workshop on Boolean Problems, Freiberg, Germany, pp. 121-125
Poretski P.S. (1884), On the Method for Solving Logical Equations and on the Inverse Methods for Mathematical Logic, Sobranie protokolov zasedanii fiz.mat., Kazan, Russia, vol. 2, pp. 161-330 (In Russain)

Pottosina S., Shmerko V., Kuzmitsky D., and Yanushkevich S. (1990), Boolean Differential Calculus in Computing, Textbook, Part 1. Matrix Tools of Boolean Differential Calculus, Preprint. Radioengineering Institute, Minsk, Belarus, 83 p. (In Russian)
Pottosina S., Shmerko V., Kuzmitsky D., and Yanushkevich S. (1991), Boolean Differential Calculus in Computing. Textbook, Part 2, Solving Some Applied Problems by Boolean Differential Calculus, Preprint, Radioengineering Institute, Minsk, Belarus, 87 p. (In Russian)
Prasanna Kumar V.K., and Tsai Y.C. (1989), Designing Linear Systolic Arrays, J. Parallel and Distributed Computing, no. 7, pp. 441-463
Rahardja S., and Falkowski B.J. (1996), Family of Fast Mixed Arithmetic Logic Transforms for Multiple-Valued Input Binary Functions, Proc. $26^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 24-29
Rasiowa H. (1975), Multiple-Valued Algorithmic Logic as a Tool to Investigate Programs, Proc. $5^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic
Reddy B.R.K., and Pail A.L. (1988), Reed-Muller Transform Image Coding, Computer Vision, Graphics, and Image Processing, vol. 42, pp. 48-61
Reed I.S. (1954), A Class of Multiple-Error-Correcting Codes and the Decoding Scheme, Trans. of IRE, no. 9. pp. 38-49
Reischke K., and Ushakov I. (1988), Estimation of Systems Reliability by Graphs, Publishing House "Radio i Sviaz", Moscow, Russia (In Russian)
Rich D.A., Naiff K.L.C., and Smalley K.G. (1985), A Four State ROM Using Multilevel Process Technology, Proc. $15^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 236-240
Rich D.A. (1986), A Survey of Multilevel Memories, IEEE Trans. Computers, vol. C-35, no. 2, pp. 99-106
Riege M.W., and Besslich Ph.W. (1992), Low-Complexity Synthesis of Incompletely Specified Multiple-Output Mod-2 Sums, IEE Proceedings, Pt.E, vol. 139, no. 4, pp. 355-362
Rine D.C. (Ed.) (1984), Computer Science and Multiple-Valued Logic. Theory and Applications. $2^{\text {nd }}$ ed. Amsterdam: North-Holland
Rooß D. 1997), Recent Developments in DNA-Computing, Proc. $27^{\text {th }}$ IEEE Int. Symp. on MultipleValued Logic, pp. 3-9
Rosser J.B., and Turquette A.R. (1952), Many-Valued Logic, $N Y$
Rosenberg I. (1974), Minimization of Pseudo-Boolean Functions by Binary Development, Discrete Math., no. 7, pp. 151-165
Roth J.P. (1966), Diagnosis of Automata Failures: A Calculus and a Method, IBM Journal Research \& Development, vol. 10. pp. 278-291
Roth J.P. (1980), Computer Logic, Testing, and Verification, Computer Science Press, Inc., Maryland, USA
Rozon C. (1988), Pseudo-Random Testing of CMOS Ternary Logic Circuits, Proc. $18^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 316-320
Rudeanu S. (1974), Boolean Functions and Equations, Noth-Holland Publishing Comp.
Rudnick E.M, Holm J.G., Saab D.G., and Patel J.H. (1994), Application of Simple Genetic Algorithms to Sequential Circuit Test Generation. Proc. European Design and Test Conf., Paris, France, pp. 40-45
Rutz R.F. (1957), Two Collector Transistor for Binary Full-addition, IBM J. Res.Develop, vol. 1. pp. 212-222.
Sapiecha K. (1987), Testowanie i Diagnostyka Systemów Cyfrowych, Państwowe Wydawnictwo Naukowe, Warszawa, 381 str. (In Polish)
Sarkar D. (1997), Operations on Binary Images Encoded as Minimized Boolean Functions, Pattern Recognition Letters, 18, pp. 455-463
Sasao T.(1989) On the Optimal Design of Multiple-Valued PLA's, IEEE Trans. Computers, vol. C-38, no. 4, pp. 582-592

Sasao T., and Besslich Ph. (1990), On the Complexity of Mod-2 sum PLA's", IEEE Trans.on Computers, vol. C-39, no. 2, pp. 262-266
Sasao T. (1992), Optimization of Multiple-Valued AND-EXOR Expressions Using Multiple-Place Decision Diagrams, Proc. $22^{\text {nd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 451-458
Sasao T. (1993a), EXMIN2: A Simplification Algorithm for Exclusive-OR-Sum-of Products Expressions for Multiple-Valued-Input Two-valued-Output Functions, IEEE Trans. ComputerAided Design of Integrated Circuits and Systems, vol. C-12, no. 5, pp. 621-632
Sasao T. (Ed.) (1993b), Logic Synthesis and Optimization, Kluwer Acad. Publ., Boston
Sasao T., and Izuhara F. (1995), Extract Minimization of Fixed Polarity Reed-Muller Expressions using Multi-terminal EXOR Ternary Decision Diagrams, Proc. IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Tokyo, pp. 213-220
Sasao T., and Fujita M. (Eds.) (1996), Representations of Discrete Functions, Kluwer Academic Publishers
Schauer P., Stewart R., Pohm A., and Reid A. (1960), Some Applications of Magnetic Film Parametron as logical Devices, IRE Transactions on Electronic Computres, vol. EC-19, pp. 315320
Scheuring R., and Wehlan H. (1991a), On the Design of Discrete Event Dynamic Systems by Means of the Boolean Differential Calculus. In book: D. Franke and F. Kraus (Eds), Design Methods of Control Systems, Pergamon Press, Oxford, pp. 463-468.
Scheuring R., and Wehlan H. (1991b), Der Boolesche Diferentialkalkul - Eine Methode zur Analyse und Synthese von Petri-Netzen, Automatisierungstechnik, vol. 39., no. H7, pp. 226-233
Schneeweiss W.G. (1996), A Necessary and Sufficient Criterion for the Monotonicity of Boolean Functions with Deterministic and Stochastic Applications, IEEE Trans. Computers, vol. C-45, no. 11, pp. 1300-1302
Schneeweiss W.G. (1989), Boolean Functions with Engineering Applications and Computer Programs, Springer-Verlag.
Schultz M.H., Trischler E., and Sarfert T.M. (1988), SOCRATES: a Highly Efficient Automatic Test Pattern Generation System, IEEE Trans. on Computer-Aided Design, vol. 7, Jan., pp. 126-137
Schröder E. (1877), Der Operationskreis des Logikkalkuls, Leipzig
Sellers F.F., Hsiao M.Y., and Bearson L.W. (1968), Analyzing Errors with the Boolean Difference, IEEE Trans. Computers, no. 1, pp. 676-683
Shin-Ichi Minato (1997), Arithmetic Boolean Expression Manipulator using BDDs, Formal Methods in System Design (Netherlands), vol. 10, pp. 221-242
Shmerko V. (1989), Synthesis of Arithmetic Forms of Boolean Functions Using the Fourier Transform, Automation and Remote Control (USA), vol. 50, no. 5, Part 2, pp. 684-691
Shmerko V., and Yanushkevich S. (1990), Algorithms of Boolean Differential Calculus for Systolic Arrays. Cybernetics, The Ukrainian Akademy of Sciences, no. 3 , pp. 38-47 (In Russian), Translated Cybernetics and System Analysis (USA)
Shmerko V., and Yanushkevich S. (1991), Processing of Binary Images by Matrix Operators of Boolean Differential Calculus and their Realization in Linear Systolic Arrays, Pattern Recognition and Image Analisys, vol. 1, no. 4, pp. 406-422
Shmerko V., and Yanushkevich S. (1993a), Fault Detection in Multivalued Logic Networks by New Type of Derivatives of Multivalued Functions. Proc. European Conf. on Circuit Theory and Design, Switzerland, pp. 643-646
Shmerko V., Yanushkevich S., and Kochergov E. (1993b), Systolic Arrays for Binary Image Processing by Using Boolean Differential Operators. Proc. Int. Conf. on High Definition Video, Germany, vol. 1976, pp. 324-335
Shmerko V., Yanushkevich S., and Levashenko V. (1996a), Techniques of Computing Logical Derivatives for MVL-functions, Proc. $26^{\text {th }}$ IEEE Int. Symp on Multiple-Valued Logic, pp. 267272

Shmerko V., Yanushkevich S., and Malecki K. (1996b), A Class of Logic Design Problems Solved Based on Parallel Computations of Butterfly Configurations, Proc. Int. Conf. on Parallel and Distributed Processing Techniques and Application, New Horizons, USA, pp. 234-240
Shmerko V., Yanushkevich S., Levashenko V., and Zaitseva E. (1996c), Test Generation for MultiValued Logic Networks by Logic Derivatives, Proc. Workshop on Design Methodologies for Signal Processing, Zakopane, Poland, pp. 319-322
Shmerko V., Yanushkevich S., and Levashenko V. (1997a), Test Pattern Generation for Combinational MVL Networks Based on Generalized D-algorithm, Proc. $27^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 139-144
Shmerko V., Holowinski G., Song N., Dill K., Ganguly K., Safranek R., Perkowski M. (1997b), HighQuality Minimization of Multi-Valued Input Binary Output Exclusive-Or Sum of Product Expressions for Strongly Unspecified Multi-Output Functions, Proc. Int. Conf. on Applications of Computer Systems, Poland, pp. 248-255
Shmerko V, Perkowski M., Rogers W., Dueck G., and Yanushkevich S. (1998), Bio-Technologies in Computing: The Promises and the Reality, Proc. Int. Conf. on Computational Inelligence and Multimedia Applications, H.Servaraj, and B.Verma (Eds), Australia, pp. 396-409
Sikorski R. (1967), Boolean Algebras, $3^{r d}$ ed. Springer Verlag, Berlin
Simovici D.A., and Reischer C. (1993), On Functional Entropy, Proc. $23^{\text {rd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 100-104
Simovici D.A. Shmerko V., Cheushev V., and Yanushkevich S. (1997), Information Estimation for Logic Functions, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 287-300
Smith K.C. (1988), Multiple-Valued Logic: Tutorial and Appreciation, IEEE Trans. Computers, vol. 21, no. 4, pp. 17-27
Song N., and Perkowski M. (1993), EXORCISM-MV-2: Minimisation of Exclusive Sum of Products Expressions for Multiple-Valued Input Incompletely Specified Functions, Proc. $23^{\text {nd }}$ IEEE Int.Symp on Multiple-Valued Logic, pp. 132-137
Song N., and Perkowski M. (1996), Minimization of Exclusive Sum of Products Expressions for Multi-Output Multiple-Valued Input, Incompletely Specified Functions, IEEE Trans. on CAD, vol. 15, no. 4, pp. 385-395
Song N., and Perkowski M. (1997), Fast Look-Ahead Algorithm for Approximate ESOP Mimimization of Incompletely Specified Multi-Output Boolean Functions, Proc. IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansions in Circuit Design, UK, pp. 61-72
Spillman R.J., and Su S.Y.H. (1977), Detection of Single, Stuck-Type Failures in Multivalued Combinational Networks, IEEE Trans. Computers, vol. C-26, no. 12, pp. 1242-1251
Srinivasan A., Kam T., Malik Sh., Brayant R.K. (1990), Algorithms for Discrete Function Manipulation, Proc. Int. Conf. on CAD, pp. 92-95
Stankovic R.S. (1991), Fast Algorithns for Calculation of Gibbs Derivatives on Finite Groups, Approx. Theory and its Appl., vol. 7, no. 2, pp. 1-19
Stankovic R.S. (1992), Some Remarks on Fourier Transforms and Differential Operators for Digital Functions, Proc. $22^{\text {nd }}$ IEEE Int.Symp on Multiple-Valued Logic, pp. 365-370
Stankovic R., Stankovic M., Moraga C., and Sasao T. (1994), Calculation of Reed-Muller-Fourier Coefficients of Multiple-Valued Functions Trough Multiple-Place Decision Diagrams, Proc. $24^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 82-87
Stankovic R.S., (1995), Functional Decision Diagrams for Multiple-Valued Functions, Proc. $25^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 284-289
Stankovic R.S., Sasao T., and Moraga C. (1996a), Spectral Transform Decision Diagrams, In book: Representations of Discrete Functions, T. Sasao (Ed.), Kluwer Academic Publishers, pp. 55-92
Stankovic R., etc. (Eds) (1996b), Recent Developments in Abstract Harmonic Analysis with Applications in Signal Processing, Belgrade, Nauka
Stankovic R.S., Stankovic M., Jankovic D., Shmerko V., and Yanushkevich S. (1997), Calculation of

Logical Derivatives Through Decision Diagram. Proc. Int. Conf. on Computer - Aided Design of Discrete Devices, Minsk, Belarus, vol. 1. pp. 46-53
Stark M. (1981), Two Bits Per Cell ROM, Proc. IEEE COMPCON, pp. 209-216
Steinbach B., and Wereszynski A. (1995), Synthesis of Multi-Level Circuits Using EXOR-Gates, Proc. IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Japan, pp. 161-168
Steinbach B., and Zhang Z. (1996), Synthesis for Full Testability of Large Partitioned Combinational Circuits, Proc. Second Int. Workshop on Boolean Problems, Germany, pp. 31-38
Strazdins I. (1983), The Polynomial Algebra of Multivalue Logic, Algebra, Combinatorics and Logic in Computer Science, 42, pp. 777-785
Tabakow I.G. (1993), Using D-Algebra to Generate Tests for $m$-Logic Combinational Circuits, Int. J. Electronics, vol. 75, no. 5, pp. 897-906
Takamatsu Y. and Kinoshita K. (1989), CONT: A Concurrent Test Generation System, IEEE Trans. on Computer-Aided Design, 8(9), pp. 966-972
Talantsev A.D. (1959), On the Analysis and Synthesis of Certain Electrical Circuits by Means of Special Logic Operators, Automatika i Telemechanika, 20, no. 7, pp. 898-907 (In Russian)
Tapia M.A., Guima T.A., and Katbab A. (1991), Calculus for a Multivalued Logic Algebraic System, Applied Mathematics and Computation, pp. 225-285
Thayse A. (1972), A Fast Algorithm for the Proper Decomposition of Boolean Functions, Philips Res. Repts., 27, pp. 140-150
Thayse A., and Davio M. (1973), Boolean Differential Calculus and its Application to Switching Theory, IEEE Trans Computers, vol. C-22, pp. 409-420
Thayse A. (1973c), Disjunctive and Conjunctive Operators for Boolean Functions, Philips Res. Repts., 28, pp. 1-16
Thayse A. (1974a), Differential Calculus for Functions from (GF(p)), Philips Res. Repts., 29, pp. 560586
Thayse A. (1974b), New Method for Obtaining the Optimal Taylor Expansions of a Boolean Function, Electronic Letters, 10, pp. 543-544
Thayse A. (1981), Boolean Calculus of Differences, Springer-Verlag, Berlin
Thompson A. (1996), An Evolved Circuit, Intrinsic in Silicon, Entwined with Physics, Lecture Notes in Computer Science, no. 1259, T.Higuchi, M.Iwata, and W.Liu (Eds), Springer-Verlag, pp. 390405
Tosic J. (1970), Arithmetical Representations of Logic Functions, In book: Discrete Automatics and Connection Networks, USSR Academy of Sciences, Nauka, Moscow, pp. 131-136 (In Russian)
Tosic Z. (1972), Analitical Representation of $m$-Valued Logical Functions over the Ring of Intergers Modulo m Doctoral Thesis, University of Nis, Yugoslavia
Tran A., and Wang J. (1993), Decomposition Method for Minimisation of Reed-Muller Polynomials in Mixed Polarity. IEE Proc.E, vol. 140, no. 1, pp. 65-68
Tucker J.H., Tapia M.A., and Bennet A.W. (1985), Boolean Integral Calculus for Digital Systems, IEEE Trans. Computers, vol. C-34, pp. 78-81
Varma D., and Trachtenberg, E.A. (1991), Computation of Reed-Muller Expansions of Incompletely Specified Boolean Functions From Reduced Representations, IEE Proc.E, vol. 138, no. 2, pp. 85-92
Varshney P.K., Hartmann C.R.P., and De Faria J.M. (1982), Application of Information Theory to Sequential Fault Diagnosis, IEEE Trans. on Computers, vol. C-31, pp. 164-170
Vranesic Z.C., Lee E.S., and Smith K.C. (1970), A Many-Valued Algebra for Switchimg Systems, IEEE Trans Computers, vol. C-19, pp 964-971
Vrudhula S.B.K., Pedram M., and Lai Y.Te (1996), EDGE Valued Binary Decision Diagrams. In book: Representations of Discrete Functions, T, Sasao and Fujita M. (Eds.), Kluwer Academic Publishers, 1996, pp. 107-132

Wang H.M., Lee C.L., and Chen J.E. (1994), Complete Test Set for Multiple-Valued Logic Networks, Proc. $24^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 289-296
Webb D.L. (1935), Generation of any N-valued Logic by One Binary Operator, Proc. Nat. Acad. Sci., vol. 21, pp. 252-254
Weixing Z. and Weiyi S. (1987), The Logical Derivatives and Integrals, J. Math. Res.\& Exposition (China), no. 2, pp. 217-224
Wesselkamper T.C. (1978), Divided Difference Method for Galois Switching Functions, IEEE Trans. Computers, vol. C-27, no. 3, pp. 232-238
Wesselkamper T.C., and Danowitz J. (1995), Some New Results for Multiple-Valued Genetic Algorithm, Proc. $25^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 264-269
Wilde D.J. (1978), Globally Optimal Design, A Wiley-Interscience Publication, John Wiley \& Sons, N.Y.

Whitney M., and Muzio J.C. (1984), Decisive Differences and Partial Differences for Stuck-at-Fault Detection in MVL Circuits, Proc. $14^{\text {th }}$ IEEE Int. Symp. on Multiple Valued Logic, pp. 321-330
Yablonsky S.V. (1958), Functional Constructions in the $k$-valued Logic, Reports of Steklov's Mathematical Institute, Russian Academy of Scinces, vol. 51, pp. 5-142 (In Russian)
Yanushkevich S. (1990), Systolic Arrays for Multivalued Logic Data Processing, In book: Algorithms and Systolic Processors for Multivalued Data Processing by Kukharev G., Shmerko V., and Zaitseva E., Publishing House "Nauka i Technika", Minsk, Belarus, pp. 157-252 (In Russian)
Yanushkevich S. (1992), Methods and Algorithms to Synthesize Parallel-Pipelining Processors for Logic Differential Calculus, A Thesis for the Degree of Doctor of Philosophy, Radioengineering Institute, Minsk, Belarus, 209 p. (In Russian)
Yanushkevich S. (1994a), Matrix Algorithms of Synthesis of Polynomial Forms for MVL-Functions, Proc. Int. Conf. on Parallel Processing and Applied Mathematics, Poland, pp. 113-122
Yanushkevich S. (1994b), Spectral and Differential Methods to Synthesize Polynomial Forms of MVL-Functions on Systolic Arrays, Proc. $5^{\text {th }}$ Int. Workshop on Spectral Techniques, C. Moraga, etc. (Eds.), Beijing, China, pp. 78-93
Yanushkevich S. (1994c), Systolic Algorithms to Synthesize Arithmetical Polynomial Forms for $k$ valued Logic Functions, Automation and Remote Control (USA), vol. 55, no. 12, Part 2, pp. 18121823
Yanushkevich S. (1994d), Developing Boolean Differential Calculus Methods for Arithmetical Logic, Automation and Remote Control (USA), vol. 55, no. 5, Part 2, pp. 715-729
Yanushkevich S. (1995a), Arithmetical Canonical Expansions of Boolean and MVL Functions as Generalized Reed-Muller Series, Proc. IFIP WG 10.5 Workshop on Applications of the ReedMuller Expansions in Circuit Design, Japan, pp. 300-307
Yanushkevich S. (1995b), Two-Dimensional Boolean Differencial Transforms as Mathematical Models of Two-Dimensional Bar Codes, Proc. Int. Conf. on Pattern Recognition \& Image Analysis, Minsk, Belarus, vol. 1, pp. 183-188
Yanushkevich S., Levashenko V., Majka E., and Wojciechowski D. (1995c), Neural Algorithm and Structure to Solve Boolean Differential Equations Logic Control Systems, Proc. Int. Symp. on Methods and Models in Automation and Robotics, Miedzyzdroje, Poland, pp. 763-768
Yanushkevich S., Kaczmarek A., Antonenko V., and Zaitseva E. (1995d), Synthesis of Arithmetical Forms of Boolean Functions on Neural Networks, Proc. XII Int. Conf. on Systems Science, Wroclaw, Poland, vol. 1, pp. 121-125
Yanushkevich S., Kaczmarek A., and Shmerko V. (1995e), Neural-based Computing of Boolean Functions Systems, Proc XII Int. Conf. on Systems Science, Wroclaw, Poland, vol. III, pp. 163167
Yanushkevich S., Shmerko V., and Wojciechowski D. (1995f), Logic Differential Equations in MVL Systems, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 123-130

Yanushkevich S. (1995g), Research Report: Development of the Technologies to Apply Logic Differential Calculus Theory, Grant no. 199-41-086, Fund of Informatization, State Univ. of Informatics \& Radioelectronics, Minsk, Belarus, 120 p. (In Russian)
Yanushkevich S. (1996a), Analogues of Boolean Differences and Differentials in Arithmetical Logic, Proc. Int.Workshop on Boolean Problems, Freiberg, Germany, pp. 114-121
Yanushkevich S., Roszak T., Malecki K., and Holowincki G. (1996b), Modern Achivements in MultiValued Lodic: Education Aspects of MVL Design, Proc. Int. Conf. on New Information Technologies in Education, V.Shmerko, J.Soldek, A.Dolgui, and S.Yanushkevich (Eds), Minsk, Belarus, vol. 1, pp. 317-327
Yanushkevich S., and Holowinski G. (1996c), Fast Heuristic Minimization of MVL Functions in Generalized Reed-Muller Domain, Proc. Int. Conf. on Applications of Computer Systems, Szczecin, Poland, pp. 57-64
Yanushkevich S. (1997a), Matrix Method to Solve Logic Differential Equations, Int. J. IEE Proc., Pt.E.- Computers and Digital Technique (UK), vol. 144, no. 5, pp. 267-272
Yanushkevich S., Levashenko V., and Moraga C. (1997b), Fault Models for Multiple-Valued Combinational Circuits, Proc. Int. Conf. on Applications of Computer System, Szczecin, Poland, pp. 309-314
Yanushkevich S. (1998), Research Report: Logic Differential Calculus Theory, Grant by Fund of Fundamental Researches, National Academy of Sciences, Task 3.2, State Univ. of Informatics \& Radioelectronics, Minsk, Belarus, 120 p. (In Russian)
Yau S.S., and Tang Y.S. (1971), An Efficient Algorithm for Generating Complete Test Sets for Combinational Logic Circuits. IEEE Trans. Computers, vol. C-20, no. 11. pp. 1245-1251
Yuminaka Y., Aoki T., and Higuchi T. (1993), Design of Set-Valued Logic Networks for WaveParallel Computing, Proc. $23^{\text {nd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 277-282
Yuminaka Y., Sasaki Y., Aoki T., and Higuchi T. (1998), Wave-Parallel Computing Systems Using Multiple-Valued Pseudo-Orthogonal Sequence, Proc. $28^{\text {nd }}$ IEEE Int. Symp. on Multiple-Valued Logic
Zakrevskij A., and Kalmykova A.Ju. (1969), The Solution of Systems of Logical Equations. In book: LYaPAS: A Programming Languge for Logic and Coding Algorithms, Academic Press, N.Y., pp. 193-206
Zakrevskij A. (1995a), Minimum Polynomial Implementation of Systems of Incompletely Specified Boolean Functions, Proc. IFIP WG 10.5 Workshop on Applications of the Reed-Muller Expansions in Circuit Design, Tokyo, pp. 250-256
Zakrevskij A., and Toropov N. (1995b), Optimizing Polynomial Implementation of Incompletely Specified Boolean Functions, Proc. Int.Conf. on Computer Aided Design of Discrete Devices, Minsk, Belarus, vol. 1, pp. 93-98
Zakrevskij A., Jaroszewicz S., and Yanushkevich S. (1996), Minimization of Reed-Muller Expansions for Systems of Incompletely Specified MVL Functions, Proc. Int. Symp. on Methods and Models in Automation and Robotics, Miedzyzdroje, Poland, vol. 3, pp. 1085-1090
Zakrevskij A. (1997a), Search Space Reducing: a Super - Fast Algorithm for Minimum AND/EXOR Implementation of Systems of Weakly Specified Boolean Functions, Proc. Int. Conf. on Pattern Recognition and Information Processing, Minsk, Belarus, vol. 1, pp. 327-331
Zakrevskij A., and Vasylkova I. (1997b), Inductive Inference in Systems of Logical Recognition in Case of Partial Data, Proc. Int.Conf. on Pattern Recognition and Information Processing, Minsk, Belarus, vol. 1, pp. 322-326
Zeng X., Perkowski M., and Dill K. (1995), Approximate Minimization of Generalized Reed-Muller Forms, Proc. IFIP WG 10.5 Workshop on Application of the Reed-Muller Canonical Expansion in Circuit Design, Japan, pp. 221-230
Zhegalkin I.L. (1928), Arithmetization of Symbolic Logic, Matematicheskij Sbornik, vol. 35, no. 1, pp. 311-373 (In Russian)

Zhegalkin I.L. (1929), Arithmetization of Symbolic Logic, Part 2, Matematicheskij Sbornik, vol. 36, no. 1, pp. 205-338 (In Russian)
Zilic Z., and Vranesic Z. (1993), Current-Mode CMOS Galois Field Circuits, Proc. $23^{\text {rd }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 245-250
Zilic Z., and Vranesic Z. (1995a), Multiple Valued Reed-Muller Transform for Incompletely Functions, IEEE Trans. Computers, vol. C-44, no. 8, pp. 1012-1020
Zilic Z., and Vranesic Z. (1995b), Reed-Muller Transform for Incompletely Specified Functions via Sparse Polynomial Interpolation, Proc. IEEE Int. Symp. on Multiple-Valued Logic, pp. 82-88
Zilic Z., and Vranesic Z. (1996), New Interpolation Algorithms for Multiple-Valued Reed- Muller Forms, Proc. $26^{\text {th }}$ IEEE Int. Symp. on Multiple-Valued Logic, pp. 16-23
Zilic Z. (1997), Towards Spectral Synthesis: Field Expansions for Partial Functions and Logic Modules for FPGAs, Doctoral thesis, University of Toronto, Canada, 154 p.

