

# Contents

## **Preface xxi**

## **1 Overview 1**

- 1.0 Introduction 1
- 1.1 Laying the Foundation 1
- 1.2 Design Decisions 2
  - 1.2.1 Number of Dimensions 2
  - 1.2.2 Type of Processing 2
  - 1.2.3 Arithmetic Format 2
  - 1.2.4 Weighting Functions 3
  - 1.2.5 Transform Length 3
  - 1.2.6 Algorithm Building Blocks 3
  - 1.2.7 Algorithm Construction 3
  - 1.2.8 DSP Chips 3
  - 1.2.9 Architectures 3
  - 1.2.10 Mapping Algorithms onto Architectures 4
  - 1.2.11 Board Decisions and Selection 4
  - 1.2.12 Test Signals and Procedures 4
- 1.3 Types of Examples 4
  - 1.3.1 Eight-Point DFT to FFT Example 5
  - 1.3.2 Algorithm Steps and Memory Maps 5
  - 1.3.3 Fifteen-Point or 16-Point  
FFT Algorithm Examples 5
  - 1.3.4 Sixteen-Point Radix-4 FFT Algorithm Examples 5
  - 1.3.5 Four-Point FFT and 16-Point Radix-4  
FFT Algorithm Examples 5

## viii CONTENTS

- 1.4 Design Examples 6
  - 1.4.1 Doppler Radar 6
  - 1.4.2 Power Spectrum Estimator 6
  - 1.4.3 Speech Recognition 6
  - 1.4.4 Image Deblurring 6
- 1.5 Conclusions 7

## **2 The Discrete Fourier Transform 9**

- 2.0 Introduction 9
- 2.1 Common Uses of the DFT 10
- 2.2 Equation and Block Diagram 10
- 2.3 Properties 10
  - 2.3.1 Frequency Limits 10
  - 2.3.2 DFT Filter Spacing/Nulls 12
  - 2.3.3 Linearity 12
  - 2.3.4 Symmetry 12
  - 2.3.5 Inverse DFT 12
  - 2.3.6 Ease of IDFT Computation 12
  - 2.3.7 Time and Frequency Scaling 13
  - 2.3.8 Time and Frequency Shifting 13
  - 2.3.9 Parseval's Theorem 14
  - 2.3.10 Zero Padding 14
  - 2.3.11 Resolution 15
  - 2.3.12 Periodicity 16
  - 2.3.13 Summary of Properties 16
- 2.4 Real Input Signals 16
  - 2.4.1 Two-Signal Algorithm 17
  - 2.4.2 Double-Length Algorithm 18
- 2.5 Strengths 20
  - 2.5.1 Periodic Signals 20
  - 2.5.2 Real or Complex Input Data 21
  - 2.5.3 Sets of Data 21
  - 2.5.4 Coherent Integration Gain 22
- 2.6 Weaknesses 22
  - 2.6.1 Computational Load 22
  - 2.6.2 Quantization Noise Error 23
  - 2.6.3 High Sidelobes 23
  - 2.6.4 Frequency Straddle Loss 23
  - 2.6.5 Transient Signals 23
- 2.7 Conclusions 24

<b>3</b>	<b>The Fast Fourier Transform</b>	<b>27</b>
3.0	Introduction	27
3.1	Improvements to the DFT	27
3.1.1	Computational Load	28
3.1.2	Quantization Noise	28
3.2	FFT-Specific Weakness	28
3.3	Eight-Point DFT to FFT Example	28
3.3.1	Eight-Point DFT Equations in Matrix Form	29
3.3.2	180° Redundant Computations	30
3.3.3	90° Redundant Computations	30
3.3.4	45° Redundant Computations	31
3.4	Building-Block Construction of FFT Algorithms	32
3.5	Conclusions	34
<b>4</b>	<b>Weighting Functions</b>	<b>35</b>
4.0	Introduction	35
4.1	Six Performance Measures	35
4.1.1	Highest Sidelobe Level	36
4.1.2	Sidelobe Fall-off Ratio	36
4.1.3	Frequency Straddle Loss	36
4.1.4	Coherent Integration Gain	36
4.1.5	Equivalent Noise Bandwidth	36
4.1.6	Three dB Main-Lobe Bandwidth	37
4.2	Weighting Function Equations and Their FFTs	37
4.2.1	Rectangular	37
4.2.2	Triangular	38
4.2.3	Sine Lobe	39
4.2.4	Hanning	40
4.2.5	Sine Cubed	40
4.2.6	Sine to the Fourth	41
4.2.7	Hamming	42
4.2.8	Blackman	43
4.2.9	Three-Sample Blackman-Harris	43
4.2.10	Four-Sample Blackman-Harris	45
4.2.11	Kaiser-Bessel	46
4.2.12	Gaussian	48
4.2.13	Dolph-Chebyshev	49
4.2.14	Finite Impulse Response Filter Design Techniques	52
4.3	Weighting Function Comparison Matrix	52
4.4	Conclusions	53

## **5 Frequency Analysis 55**

- 5.0 Introduction 55
- 5.1 Five Performance Measures 55
  - 5.1.1 Input Sample Overlap 55
  - 5.1.2 Sidelobe Level 56
  - 5.1.3 Frequency Straddle Loss 56
  - 5.1.4 Frequency Resolution 56
  - 5.1.5 Coherent Integration Gain 57
- 5.2 Computational Techniques 57
  - 5.2.1 Nonoverlapped 57
  - 5.2.2 Overlapped 58
  - 5.2.3 Weighting Functions 58
- 5.3 Conclusions 59

## **6 Linear Filtering and Pattern Matching 61**

- 6.0 Introduction 61
- 6.1 Equations 61
- 6.2 Three Performance Measures 62
  - 6.2.1 Number of Computations per Data Point 62
  - 6.2.2 Number of Data Memory Locations 62
  - 6.2.3 Computational Latency 63
- 6.3 Direct Method 63
  - 6.3.1 Complex Input Signal 63
  - 6.3.2 Real Input Signal 63
- 6.4 Single-Step Frequency Domain Method 64
  - 6.4.1 Complex Input Signal 64
  - 6.4.2 Real Input Signal 64
- 6.5 Multiple-Step Frequency Domain Method 65
- 6.6 Overlap-and-Add Frequency Domain Algorithm 65
  - 6.6.1 Introduction 65
  - 6.6.2 Complex Input Signals 65
  - 6.6.3 Real Input Signals 67
- 6.7 Overlap-and-Save Frequency Domain Algorithm 68
  - 6.7.1 Introduction 68
  - 6.7.2 Complex Input Signals 69
  - 6.7.3 Real Input Signals 70
- 6.8 Linear Filtering and Pattern Matching
  - Comparison Matrix 70
- 6.9 Conclusions 71

**7 Multidimensional Processing 73**

- 7.0 Introduction 73
- 7.1 Frequency Analysis 74
  - 7.1.1 Two Dimensions 74
  - 7.1.2 Three or More Dimensions 75
- 7.2 Linear Filtering 75
  - 7.2.1 Separable Two-Dimensional Filter 76
  - 7.2.2 Frequency Domain Approach 76
  - 7.2.3 Three and More Dimensions 77
- 7.3 Pattern Matching 78
  - 7.3.1 Separable Two-Dimensional Pattern Matching 78
  - 7.3.2 Frequency Domain Approach 79
  - 7.3.3 Three and More Dimensions 80
- 7.4 Conclusions 80

**8 Building-Block Algorithms 81**

- 8.0 Introduction 81
- 8.1 Four Performance Measures 81
  - 8.1.1 Number of Adds 82
  - 8.1.2 Number of Multiplies 82
  - 8.1.3 Number of Memory Locations for  
Multiplier Constants 82
  - 8.1.4 Number of Data Memory Locations 83
- 8.2 Ten Building-Block Algorithm Constraints 83
- 8.3 Two-Point FFT 84
- 8.4 Three-Point FFT 85
  - 8.4.1 Winograd 3-Point FFT 85
  - 8.4.2 Singleton 3-Point FFT 86
- 8.5 Four-Point FFT 87
- 8.6 Five-Point FFT 88
  - 8.6.1 Winograd 5-Point FFT 89
  - 8.6.2 Singleton 5-Point FFT 91
  - 8.6.3 Rader 5-Point FFT 93
- 8.7 Seven-Point FFT 96
  - 8.7.1 Winograd 7-Point FFT 97
  - 8.7.2 Singleton 7-Point FFT 101
- 8.8 Eight-Point FFT 103
  - 8.8.1 Winograd 8-Point FFT 104
  - 8.8.2 Eight-Point Radix-4 and -2 Algorithm 107
  - 8.8.3 Eight-Point Radix-2 Algorithm 110
  - 8.8.4 PTL 8-Point FFT 113

- 8.9 Nine-Point FFT 116
  - 8.9.1 Winograd 9-point FFT 116
  - 8.9.2 PTL 9-point FFT 121
  - 8.9.3 Burrus and Eschenbacher 9-point FFT 124
- 8.10 Sixteen-Point FFT 128
  - 8.10.1 Winograd 16-point FFT 128
- 8.11 General Algorithms for All Odd Numbers 136
  - 8.11.1 General Rader Algorithm 136
  - 8.11.2 General Singleton Algorithm 138
  - 8.11.3 General SWIFT Odd-Point Algorithm 140
- 8.12 Building-Block Algorithm Comparison Matrix 142
- 8.13 Conclusions 142

## **9 Algorithm Construction 145**

- 9.0 Introduction 145
- 9.1 Four Performance Measures 145
  - 9.1.1 Number of Adds 146
  - 9.1.2 Number of Multiplies 146
  - 9.1.3 Number of Memory Locations  
for Multiplier Constants 146
  - 9.1.4 Number of Data Memory Locations 146
- 9.2 Nine Algorithm Constraints 146
- 9.3 Three Construction Approaches 147
- 9.4 Algorithm Data Mapping Relabeling 148
  - 9.4.1 General Address Relabeling 148
  - 9.4.2 Four-Point FFT Address Relabeling Example 148
- 9.5 Convolution Approach 149
  - 9.5.1 Bluestein Algorithm Introduction 149
  - 9.5.2 Number of Bluestein Algorithm  
Adds and Multiplies 151
  - 9.5.3 Number of Bluestein Algorithm  
Memory Locations 151
  - 9.5.4 General Bluestein Algorithm 152
  - 9.5.5 Fifteen-Point Bluestein Example 158
  - 9.5.6 Winograd Algorithm Introduction 167
  - 9.5.7 Number of Winograd Algorithm  
Adds and Multiplies 169
  - 9.5.8 General Winograd Algorithm 169
  - 9.5.9 Fifteen-Point Winograd Algorithm Example 173
- 9.6 Prime Factor Approach 185
  - 9.6.1 Prime Factor Algorithm Introduction 185
  - 9.6.2 Number of Prime Factor Algorithm  
Adds and Multiplies 187

9.6.3	General Prime Factor Algorithm for Two Factors	187
9.6.4	Fifteen-Point Kolba-Parks FFT Example	191
9.6.5	Fifteen-Point SWIFT Example	199
9.7	Mixed-Radix Approach	207
9.7.1	Mixed-Radix Algorithm Introduction	207
9.7.2	Number of Mixed-Radix Algorithm Adds and Multiplies	210
9.7.3	Categories of the Mixed-Radix Algorithm	211
9.7.4	General Mixed-Radix Algorithm for Two Factors	211
9.7.5	Sixteen-Point Radix-4 Primes-to-a-Power FFT Example	213
9.7.6	Sixteen-Point Radix-8 and -2, Mixed Power-of-Primes Example	222
9.7.7	Fifteen-Point Singleton Mixed-Radix FFT Example	230
9.8	Comparison Matrices	242
9.9	Conclusions	243
<b>10</b>	<b>Arithmetic Building Blocks for Architectures</b>	<b>245</b>
10.0	Introduction	245
10.1	Five Performance Measures	246
10.1.1	Input Data Organization	246
10.1.2	Output Data Organization	246
10.1.3	Internal Data Bus Loading	246
10.1.4	Throughput from Computations	246
10.1.5	Latency from Computations	247
10.2	Bit-Slice Arithmetic	247
10.2.1	Multiplier	248
10.2.2	Multiplier-Accumulator	250
10.3	Integrated Arithmetic	250
10.3.1	Multiplier	250
10.3.2	Multiplier-Accumulator	250
10.4	Special Purpose	251
10.4.1	FFT Data Separation Patterns	251
10.4.2	Decimation-in-Time Building Block	253
10.4.3	Decimation-in-Frequency Building Block	253
10.5	Conclusions	254
<b>11</b>	<b>Multiprocessor Architectures</b>	<b>255</b>
11.0	Introduction	255
11.1	Two Single Processors	255
11.1.1	Von Neumann Architecture	256
11.1.2	Harvard Architecture	257

- 11.2 Three Linear Arrays 258
  - 11.2.1 Pipeline 258
  - 11.2.2 Linear Bus 259
  - 11.2.3 Ring Bus 260
- 11.3 Three Parallel Arrays 262
  - 11.3.1 Crossbar 262
  - 11.3.2 Massively Parallel 264
  - 11.3.3 Star 267
- 11.4 Three Multidimensional Arrays 268
  - 11.4.1 Hypercube 269
  - 11.4.2 Massively Parallel 270
  - 11.4.3 Hybrids 270
- 11.5 Conclusions 272

## **12 Algorithm and Data Mappings 273**

- 12.0 Introduction 273
- 12.1 Five Performance Measures 273
  - 12.1.1 Input Data Overhead 274
  - 12.1.2 Intermediate Results Reorganization Overhead 274
  - 12.1.3 Output Data Overhead 274
  - 12.1.4 Computational Throughput 274
  - 12.1.5 Processing Latency 274
- 12.2 Mappings 274
- 12.3 Single Processor 275
  - 12.3.1 Data I/O Requirements 276
  - 12.3.2 Memory Requirements 276
  - 12.3.3 Arithmetic Unit Requirements 277
  - 12.3.4 Von Neumann Architecture 277
  - 12.3.5 Harvard Architecture 278
  - 12.3.6 Harvard 16-Point Radix-4 FFT Example 279
- 12.4 Three Linear Arrays 279
  - 12.4.1 Pipeline 279
  - 12.4.2 Linear Bus 283
  - 12.4.3 Ring Bus 283
  - 12.4.4 Pipeline 16-Point Radix-4 Example 284
  - 12.4.5 Linear and Ring Bus 16-Point Radix-4  
FFT Examples 286
- 12.5 Three Parallel Arrays 287
  - 12.5.1 Crossbar 16-Point Radix-4 FFT Examples 288
  - 12.5.2 Massively Parallel 16-Point Radix-4  
FFT Examples 293
  - 12.5.3 Star 16-Point Radix-4 FFT Examples 300



- 12.6 Three Multidimensional Arrays 304
  - 12.6.1 Hypercube 16-Point Radix-4 FFT Examples 305
  - 12.6.2 Massively Parallel 16-Point Radix-4  
FFT Examples 312
  - 12.6.3 Hybrid 16-Point Radix-4 FFT Examples 313
- 12.7 Algorithm Mapping Examples  
Comparison Matrix 313
- 12.8 Conclusions 313

## **13 Arithmetic Formats 315**

- 13.0 Introduction 315
- 13.1 Three Performance Measures 315
  - 13.1.1 Dynamic Range 316
  - 13.1.2 Arithmetic Accuracy 316
  - 13.1.3 Quantization Noise Escalation 316
- 13.2 Three Arithmetic Formats 316
  - 13.2.1 Fixed-Point 317
  - 13.2.2 Floating-Point 318
  - 13.2.3 Block-Floating-Point 320
- 13.3 Arithmetic Format Comparison Matrix 321
- 13.4 Conclusions 322

## **14 Chips 323**

- 14.0 Introduction 323
- 14.1 Five FFT Performance Measures 324
  - 14.1.1 1024-Point Complex FFT 324
  - 14.1.2 Data I/O Ports 324
  - 14.1.3 On-Chip Data Memory Words 325
  - 14.1.4 On-Chip Program Memory Words 325
  - 14.1.5 Number of Address Generators 325
- 14.2 Generic Programmable DSP Chip 325
  - 14.2.1 Block Diagram 326
  - 14.2.2 On-Chip Data Memory 326
  - 14.2.3 On-Chip Program Memory 327
  - 14.2.4 On-Chip Data Buses 327
  - 14.2.5 Off-Chip Data Bus 327
  - 14.2.6 On-Chip Address Buses 328
  - 14.2.7 Off-Chip Address Bus 328
  - 14.2.8 Address Generators 328
  - 14.2.9 Serial I/O Ports 329
  - 14.2.10 Program Control 332

	14.2.11	Multiplier-Accumulator and Arithmetic Logic Unit	332
	14.2.12	Estimating FFT Performance	334
14.3		Programmable Fixed-Point Chip Families	335
	14.3.1	Analog Devices ADSP-21xx Family	336
	14.3.2	AT&T DSP16 Family	338
	14.3.3	AT&T DSP161x Family	339
	14.3.4	Motorola DSP56001 Family	341
	14.3.5	Motorola DSP561xx Family	343
	14.3.6	NEC $\mu$ PD77xxx Family	344
	14.3.7	NEC $\mu$ PD7701x Family	346
	14.3.8	NEC $\mu$ PD77220 Family	347
	14.3.9	Texas Instruments TMS320C1x Family	348
	14.3.10	Texas Instruments TMS320C2x Family	350
	14.3.11	Texas Instruments TMS320C5x Family	351
	14.3.12	Zilog Z89Cxx Family	353
	14.3.13	Zoran ZR38000 Family	354
14.4		Programmable Fixed-Point Chips Comparison Matrix	355
14.5		Programmable Floating-Point Chips	357
	14.5.1	Analog Devices 21020 Family	357
	14.5.2	Analog Devices ADSP-21060 Family	358
	14.5.3	AT&T DSP32C Family	359
	14.5.4	Intel i860 Family	361
	14.5.5	Motorola DSP96002 Family	363
	14.5.6	NEC $\mu$ PD77240/230A Family	364
	14.5.7	Texas Instruments TMS320C3x Family	365
	14.5.8	Texas Instruments TMS320C40 Family	367
14.6		Programmable Floating-Point Chips Comparison Matrix	369
14.7		FFT-Specific Chips and Chip Sets	369
	14.7.1	Array Microsystems a66110/66210 Chip Set	370
	14.7.2	Sharp LH9124/LH9320 Chip Set	372
	14.7.3	Raytheon TMC2310 Chip	373
	14.7.4	Plessey Semiconductor PDSP16510 Chip	374
14.8		FFT-Specific Chip and Chip Set Comparison Matrix	375
14.9		Application-Specific Integrated Circuits	376
	14.9.1	DSP Semiconductor Pine/Oak Core Family	376
14.10		ASIC Programmable DSP Chip Cores Comparison Matrix	377

14.11	Multiple Processors on a Single Chip	378
14.11.1	Star Semiconductor SPROC-1000 Family	378
14.11.2	Texas Instruments TMS320C8x Family	381
14.12	Multiple-Processor Programmable DSP Chips Comparison Matrix	382
14.13	Conclusions	383
<b>15</b>	<b>Board Decisions and Selection</b>	<b>387</b>
15.0	Introduction	387
15.1	Five Board Selection Categories	387
15.1.1	Algorithm Performance	388
15.1.2	I/O Performance	388
15.1.3	Software Support	388
15.1.4	Expansion Capability	388
15.1.5	Multiprocessing	388
15.2	Board Selection Questions and Answers	388
15.3	Conclusions	393
<b>16</b>	<b>Test</b>	<b>395</b>
16.0	Introduction	395
16.1	Example	395
16.2	Errors during Algorithm Development	395
16.2.1	Arithmetic Check	397
16.2.2	Memory Map Check	399
16.3	Errors during Code Development	400
16.3.1	Coding the Building-Block Algorithm	400
16.3.2	Coding the Multiplier Constants	401
16.3.3	Coding the Memory Mapping	401
16.3.4	Coding the Relabeled Memory Maps	402
16.4	Errors during Product Operation	402
16.4.1	Arithmetic Unit	402
16.4.2	Address Generator	403
16.4.3	Data Memory	403
16.4.4	Program Memory	404
16.4.5	Data I/O	404
16.5	Test Signal Features	404
16.5.1	Unit Pulse	404
16.5.2	Constants	405
16.5.3	Single Sine Waves	406
16.5.4	Pair of Sine Waves	406

- 16.6 Test Signal Error Patterns 406
  - 16.6.1 Unit Pulse 407
  - 16.6.2 Constants 408
  - 16.6.3 Single Sine Waves 408
  - 16.6.4 Pair of Sine Waves 409
- 16.7 Isolating Errors: A 16-Point Example 409
  - 16.7.1 Assumptions 409
  - 16.7.2 Test Signal Strategy 410
  - 16.7.3 Error Isolation 410
- 16.8 Conclusions 412

## **17 Design Examples 413**

- 17.0 Introduction 413
- 17.1 Example 1: Doppler Radar Processor 414
  - 17.1.1 Definition of the Product 414
  - 17.1.2 Specification 414
  - 17.1.3 Description 415
  - 17.1.4 Design Decisions 416
  - 17.1.5 Board Selection Process 422
  - 17.1.6 Test Signals 423
  - 17.1.7 Design Decisions Summary 423
- 17.2 Example 2: Power Spectrum Estimator 424
  - 17.2.1 Definition of the Product 424
  - 17.2.2 Specification 424
  - 17.2.3 Description 425
  - 17.2.4 Design Decisions 427
  - 17.2.5 Board Selection Process 430
  - 17.2.6 Test Signals 430
  - 17.2.7 Design Decision Summary 431
- 17.3 Example 3: Speech Analyzer 431
  - 17.3.1 Definition of the Product 432
  - 17.3.2 Specification 432
  - 17.3.3 Description 432
  - 17.3.4 Design Decisions 435
  - 17.3.5 Board Selection Process 438
  - 17.3.6 Test Signals 439
  - 17.3.7 Design Decision Summary 439
- 17.4 Example 4: Image Deblurring 440
  - 17.4.1 Definition of the Product 440
  - 17.4.2 Specification 441
  - 17.4.3 Description 441
  - 17.4.4 Design Decisions 443

17.4.5 Board Selection Process 447  
17.4.6 Test Signals 447  
17.4.7 Design Decision Summary 447  
17.5 Conclusions 448

**Glossary 449**

**Appendix: Table of Comparison Matrices 455**

**Index 457**