Broadcast Transmission

Programmable Solutions for the Broadcast Industry

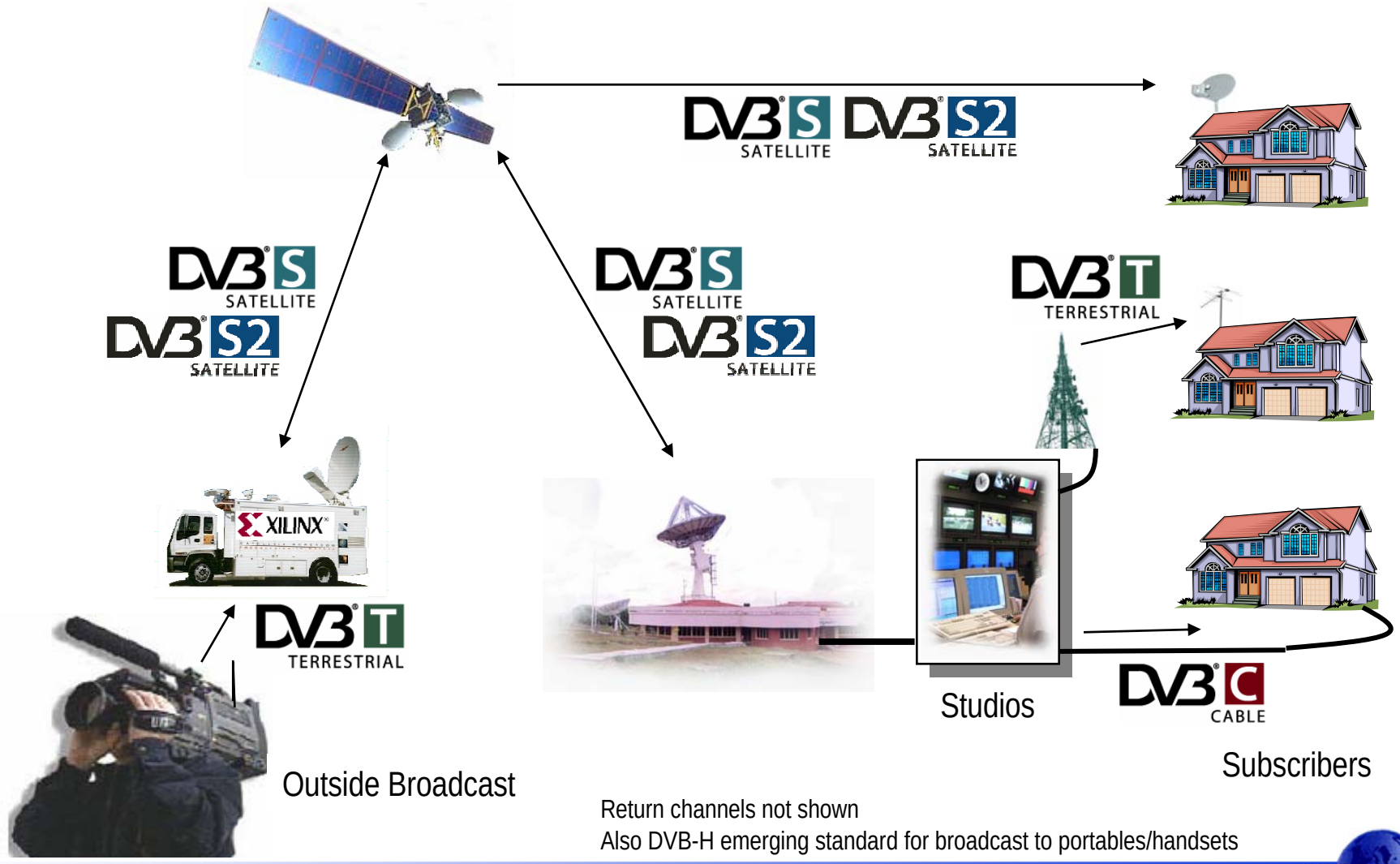
Broadcasting Standards

- Many standards across the world, existing and emerging, with just a few shown here
- However, each transmission scheme based on similar models
  - Parameterised FEC and modulation blocks will cover most requirements
- Some major standards highlighted in this presentation - contact Xilinx for more details on others

Introduction to DVB

- Digital Video Broadcasting organisation
- Formed in September 1993
- DVB now has more than 300 members
  - Broadcasters
  - Manufacturers
  - Network operators
  - Regulatory bodies
- Mission : *"The creation of a harmonious digital broadcast market for all service delivery media"*
- Mainly covers Europe but also promoting in U.S. and Japan
- Competes against ATSC (U.S.) and ISDB (Japan)

DVB in the Broadcast Chain



Return channels not shown

Also DVB-H emerging standard for broadcast to portables/handsets

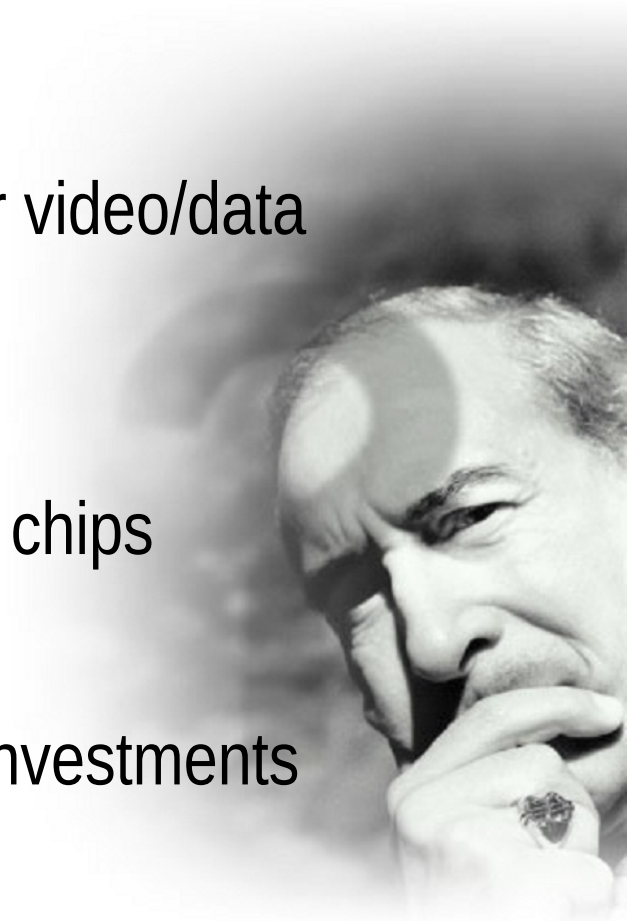
Introduction to ATSC

- Advanced Television Systems Committee
- Formed in September 1982
- ATSC currently has around 200 members
  - Broadcasters
  - Manufacturers
  - Network operators
  - Regulatory bodies

- Co-ordinates television standards among different communications media focusing on digital television, interactive systems, and broadband multimedia communications. Also developing digital television implementation strategies
- Adopted by U.S., Canada, S. Korea, Taiwan and Argentina

Issues & Requirements

- Higher throughput
  - Particularly in cable networks, higher video/data bandwidth required
- Lower cost-per-channel
  - Support for multiple channels in less chips
- Fast time-to-market
  - Need to recoup huge infrastructure investments as soon as possible



DVB Standards for Broadcast

• DVB-S (Satellite)	EN 300 421
• DVB-C (Cable)	EN 300 429
• DVB-T (Terrestrial)	EN 300 744
• DVB-S2 (2nd Generation Satellite)	EN 302 307
• DVB-CS (Satellite Master Antenna TV/SMATV)	EN 300 473
• DVB-MS (Multipoint Video Distribution Systems/MVDS)	EN 300 748
• DVB-MC (Microwave Multipoint Distribution Systems/MMDS)	EN 300 749
• DVB-SI (Service Information)	EN 300 468
• DVB-TXT (Teletext)	EN 300 472
• DVB-MHP (Multimedia Home Platform)	TS 101 812

- 100 specifications/guidelines documents FOC from ETSI (including revisions)

ATSC Broadcast Standards

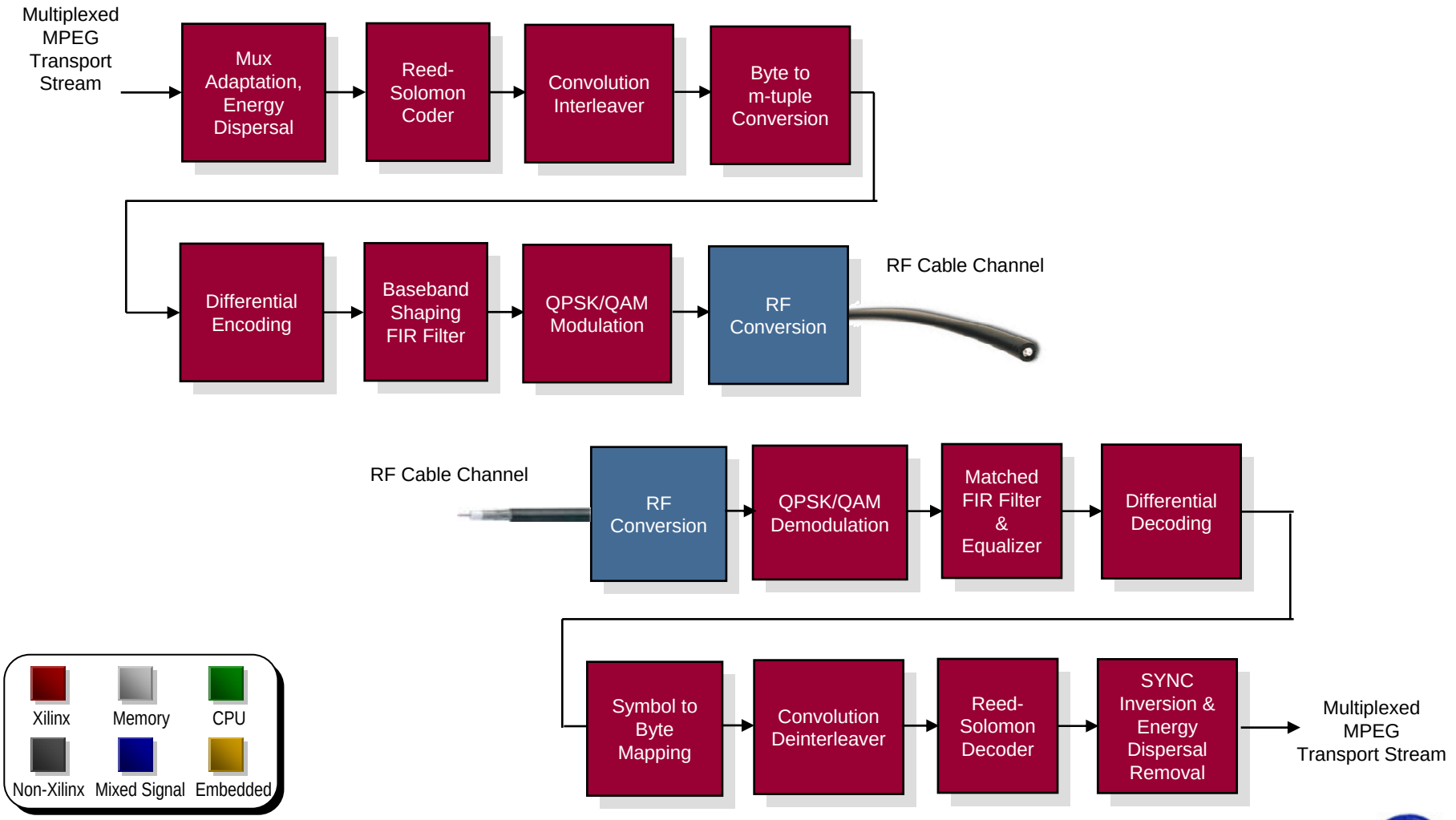
• ATSC Digital Television Standard	ATSC Document A/53B
• Digital Audio Compression (AC-3) Standard	ATSC Document A/52A
• Transmission Measurement and Compliance for Digital TV	ATSC Document A/64A
• Conditional Access System for Terrestrial Broadcast	ATSC Document A/70
• Modulation & Coding Requirements for DTV Apps Over Satellite	ATSC Document A/80
• Data Broadcast Standard	ATSC Document A/90
• Delivery of IP Multicast Sessions over Data Broadcast Standard	ATSC Document A/92

- Around 20 specifications/guidelines documents free of charge from ATSC (inc. revisions)
- This presentation focuses solely on standard A/53B
  - ATSC Digital Television Standard

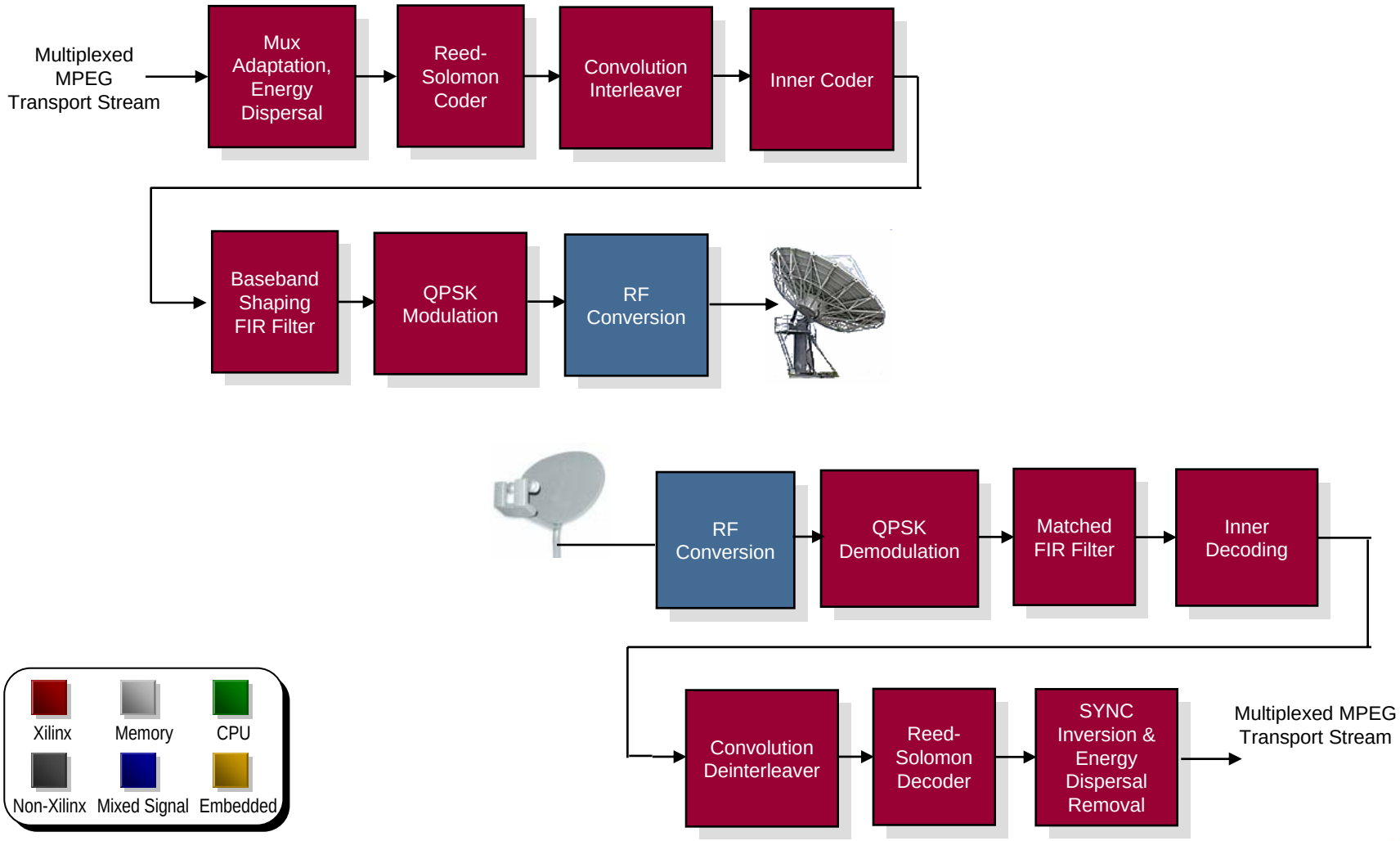
DVB/ATSC Features

- Cable
  - High bitrate, stationary receivers
  - High bitrate interactivity
  - Interactivity mostly using cable modem
  - 8MHz cable channel with DVB-C gives approx 38-40MBits/s
  - 6MHz cable channel with ATSC gives 38.57MBits/s
- Satellite
  - High bitrate, stationary receivers
  - Low bitrate interactivity currently
  - Interactivity mostly using PSTN although DVB-RCS (Return Channel for Satellite) is emerging
  - 36 MHz satellite transponder with DVB-S gives approx 40MBits/s
- Terrestrial
  - Medium or low bitrate, portable or mobile receivers
  - Low bit-rate interactivity
  - Interactivity mostly using PSTN, but DVB-T return channel systems may appear
  - 8MHz terrestrial channel with DVB-T offers around 4-27 MBits/s

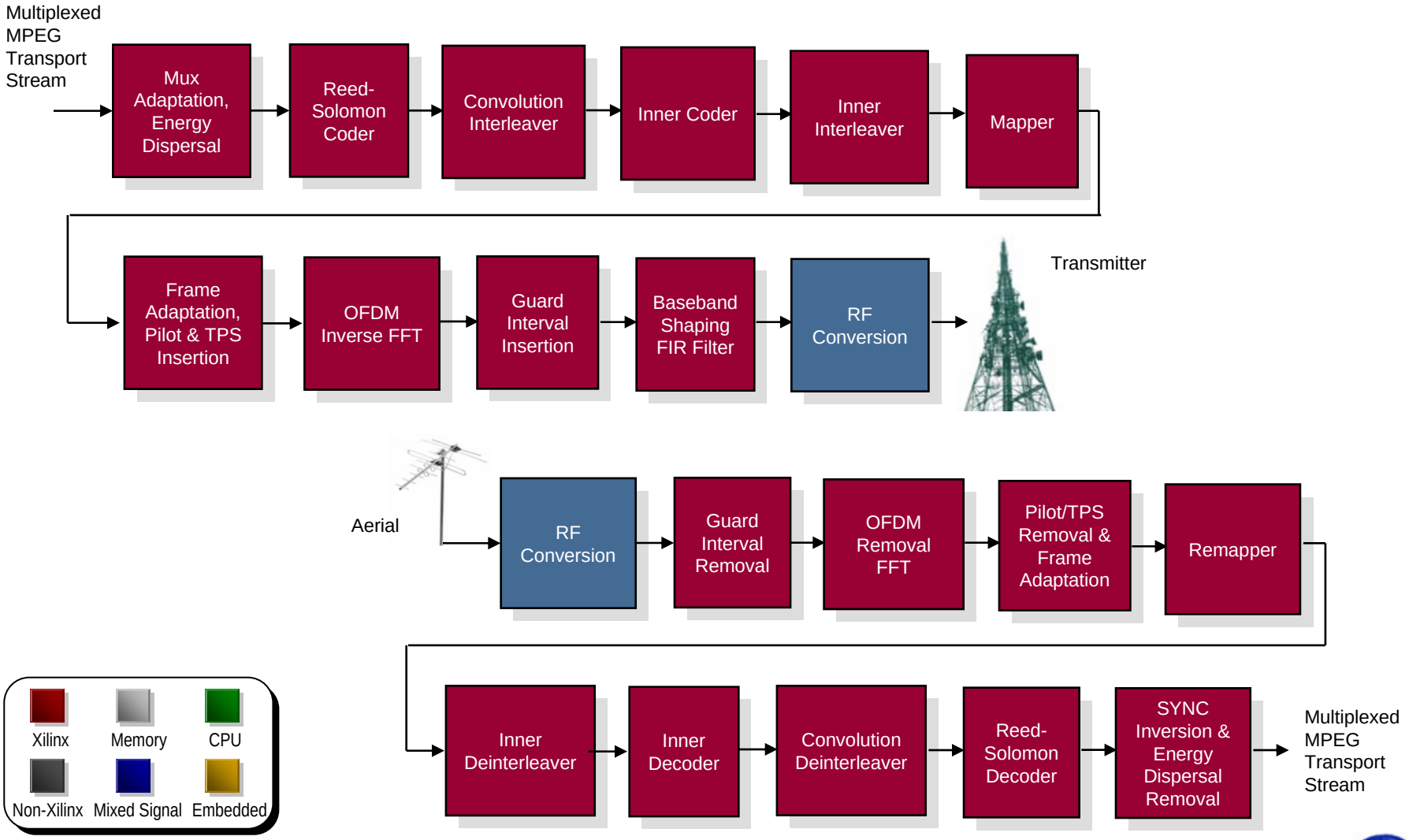
DVB-C Transmitter/Receiver



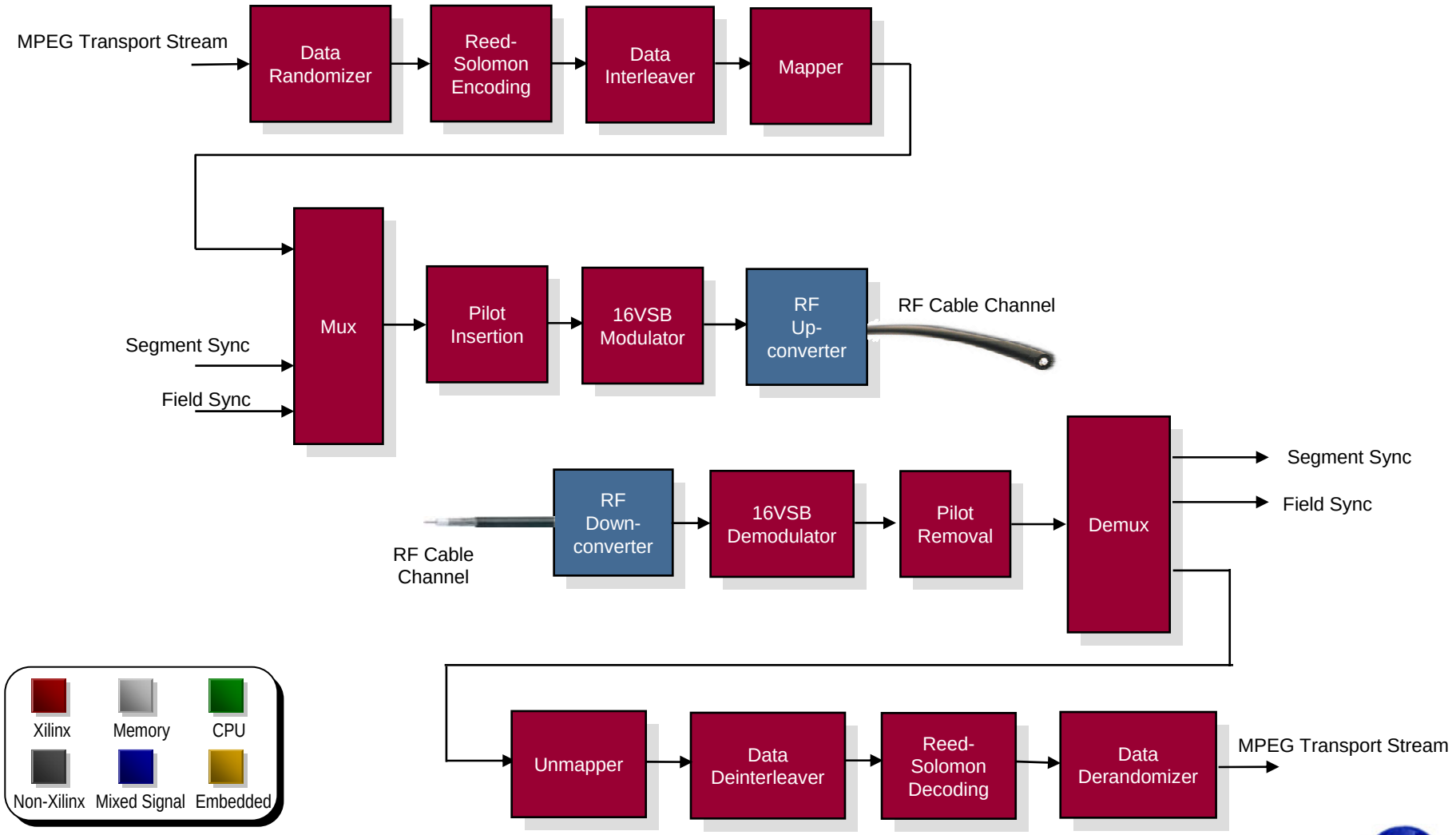
DVB-S Transmitter/Receiver



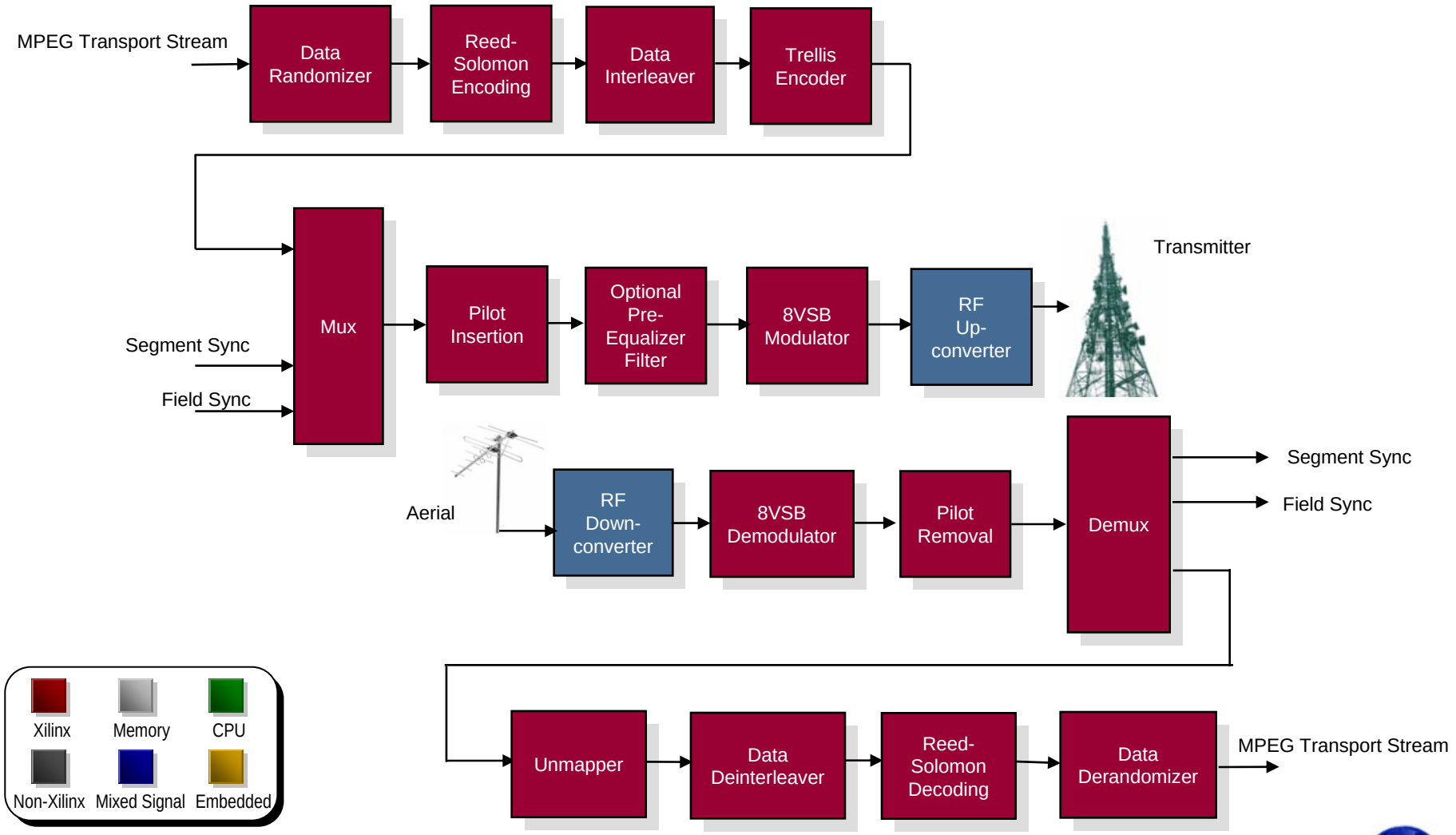
DVB-T Transmitter/Receiver



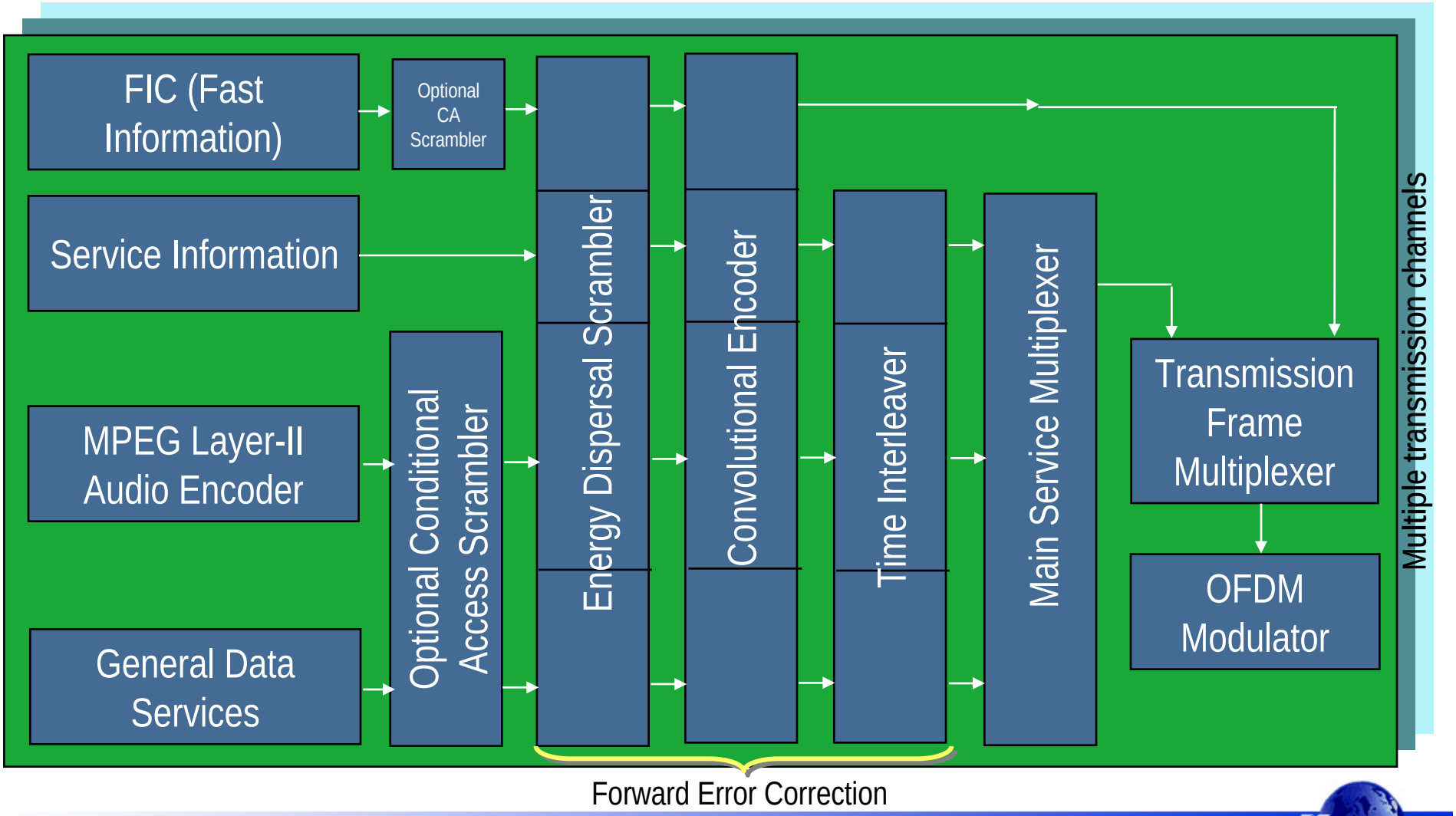
ATSC Cable Tx/Rx



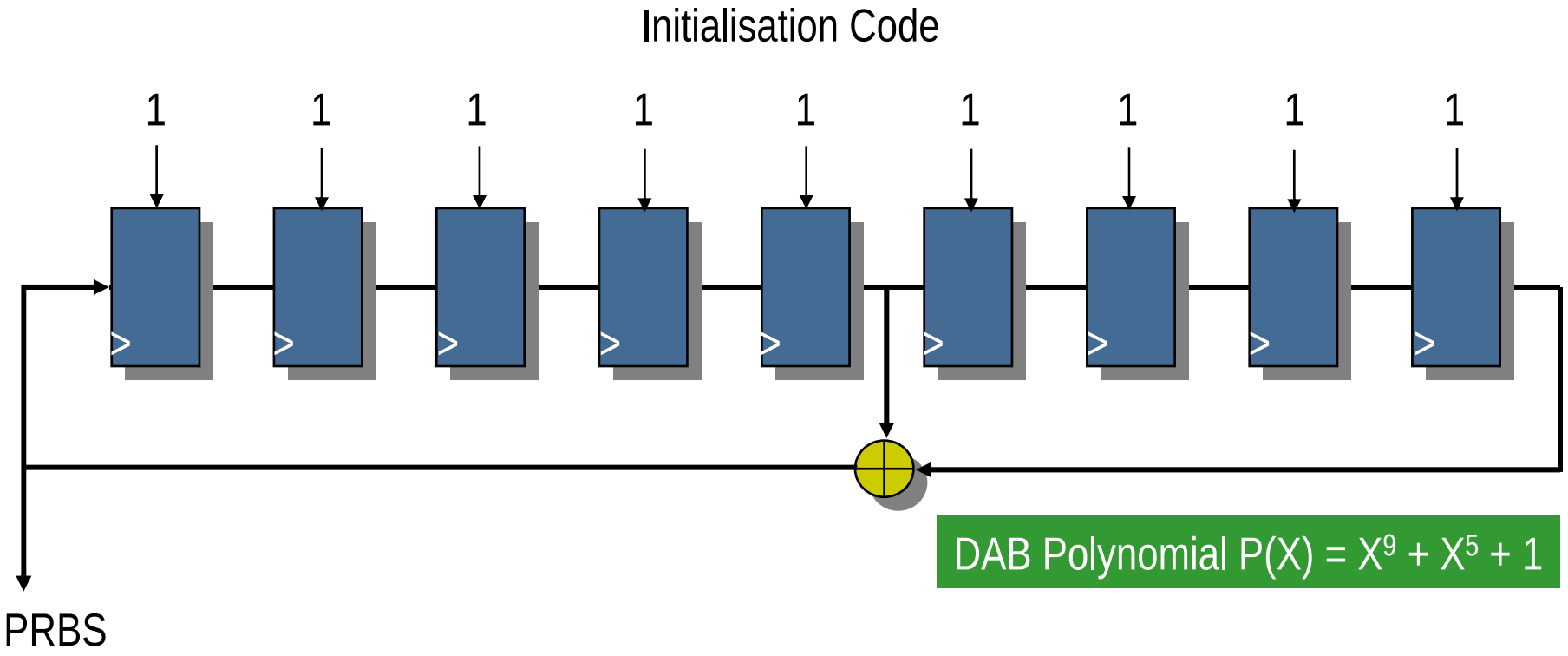
ATSC Terrestrial Tx/Rx



Basic DAB Transmitter

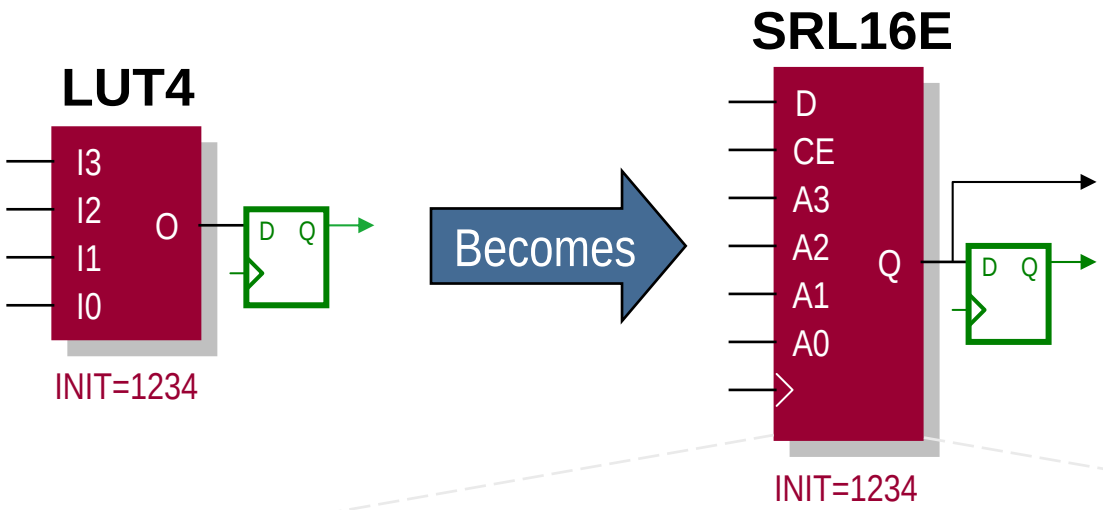


Energy Dispersal Scramblers

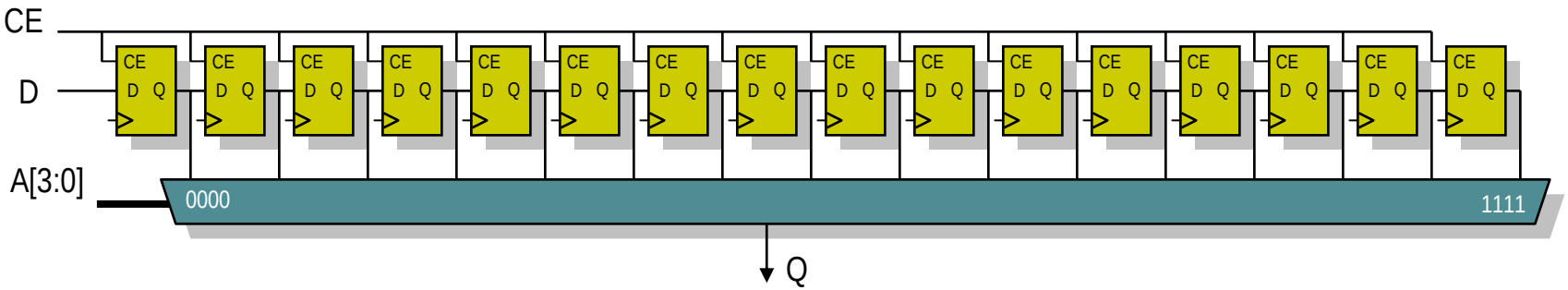


- Ensures that ratio of 0's and 1's transmitted is fairly equal
- Negligible FPGA resource (1 or 2 CLBs)
  - Particularly with use of SRL16E

Shift Register LUT - SRL16E

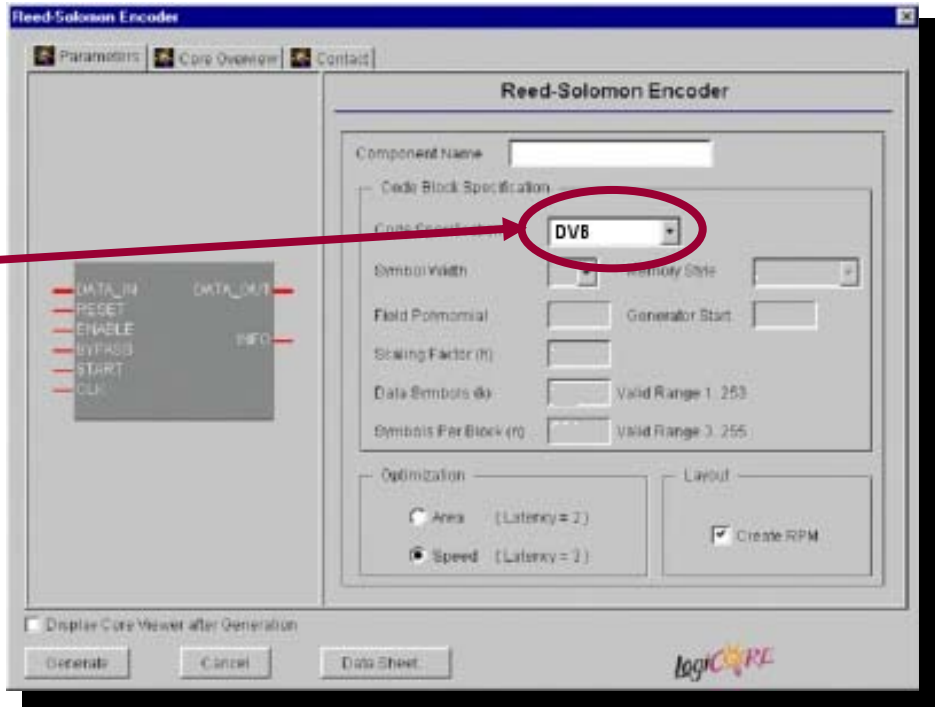


- Reading of flip-flop contents is completely independent
  - Address selects which flip-flop is read
- Read process is asynchronous, but dedicated flip-flop is available for synchronization



Xilinx Reed-Solomon

- Parameterizable encoder and decoder cores available from Xilinx
- Select DVB or ATSC from the *Code Specification* menu
- Reed-Solomon tutorials online at Xilinx IP Centre
  http://www.xilinx.com/ipcenter
- Incorporates Smart-IP



LogiCORE Reed-Solomon

Xilinx R-S Features

Reed-Solomon

Encoder

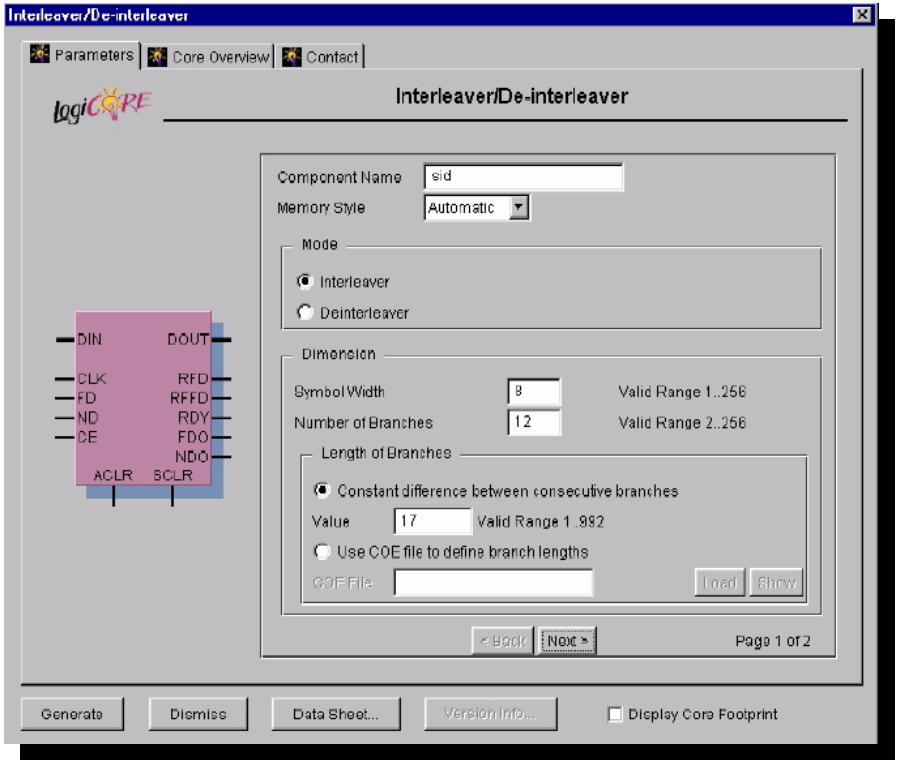
Features	ATSC 1	DVB 1
Symbol Width	N/A	N/A
Generator Start	0	0
h	1	1
k	187	188
n	207	204
Field Polynomial	285	285
Optimization	Speed	Speed
Create RPM	No	No
Xilinx Device	X2VP2-FG256-7	X2VP2-FG256-7
Use IOB Flip-Flop	Yes	Yes
Area (Slices)	121	109
Slices Remaining	1287	1299
Block Memory	0	0
Latency	3	3
Maximum Clock Frequency	311 MHz	299 MHz

Decoder

Features	ATSC 1	DVB 1
Generator Start	0	0
h	1	1
k	187	188
n	207	204
Polynomial	285	285
Symbol Width	8	8
Sync Mode	Start Pulse	Start Pulse
Clock Enable	No	No
Synochronous Reset	No	No
Delayed Original Data	No	No
Erasure Decoding	No	No
Optimization	Area	Area
Clock Periods Per Symbol	1	1
Memory Style	Automatic	Automatic
Processing Delay	294	204
Latency	507	414
Xilinx Device	2VP2-FG256-7	2VP2-FG256-7
Area (Slices)	783	618
Slices Remaining	625	790
Block Memories	2	2
Maximum Clock Frequency	126 MHz	128 MHz

Xilinx Interleaver/Deinterleaver

- Forney convolutional type architecture
- Parameterizable number of branches and branch lengths
- Symbol size from 1 to 256 bits
- Incorporates Smart-IP
- More info at http://www.xilinx.com/ipcenter



LogiCORE Interleaver/ De-interleaver

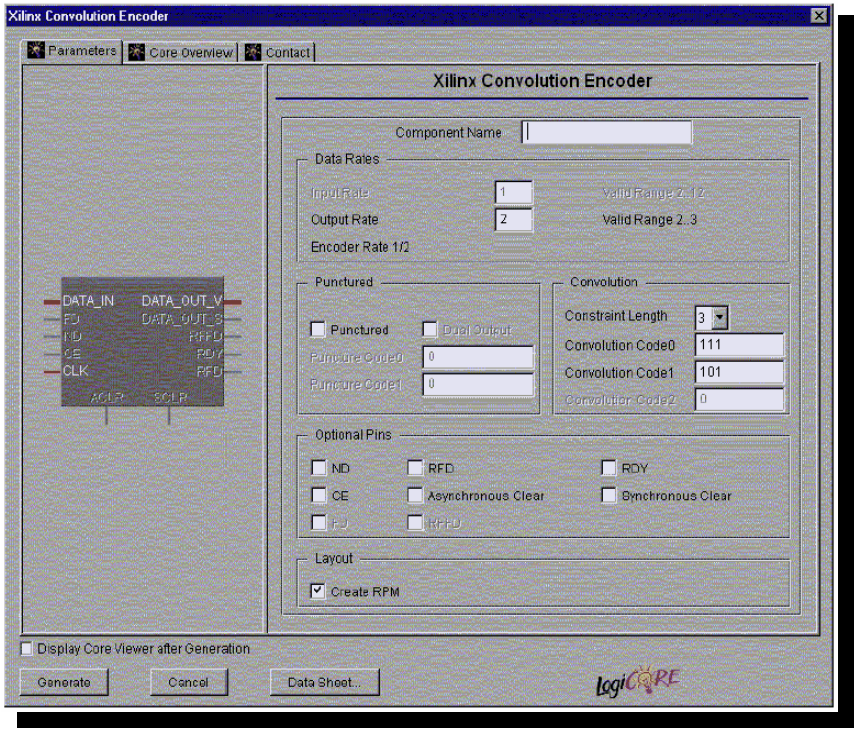
Xilinx (De)Interleaver Features

Interleaver/ De-interleaver

Options	DVB 1	DVB 2
Mode	Interleaver	De-interleaver
Number of Branches	12	12
Branch Length Constant	17	17
Symbol Width	8	8
Pipelining	Maximum	Maximum
Optional Pins	FDO, RDY, RFFD	FDO, RDY, RFFD
Memory Style	Automatic	Automatic
Create RPM	No	No
Xilinx Device	XC2V40-6	XC2V40-6
Use IOB Flip-Flops	No	No
Area (slices)	80	109
Number of Block RAMs	1	2
Maximum Clock Frequency	208 MHz	187 MHz

Xilinx Convolutional Encoder

- Parameterizable constraint length from 3 to 9
- Parameterizable convolutional codes and puncture codes
- Puncturing Rates from 2/3 to 12/13
- Incorporates Smart-IP
- More info at http://www.xilinx.com/ipcenter



LogiCORE Convolutional Encoder

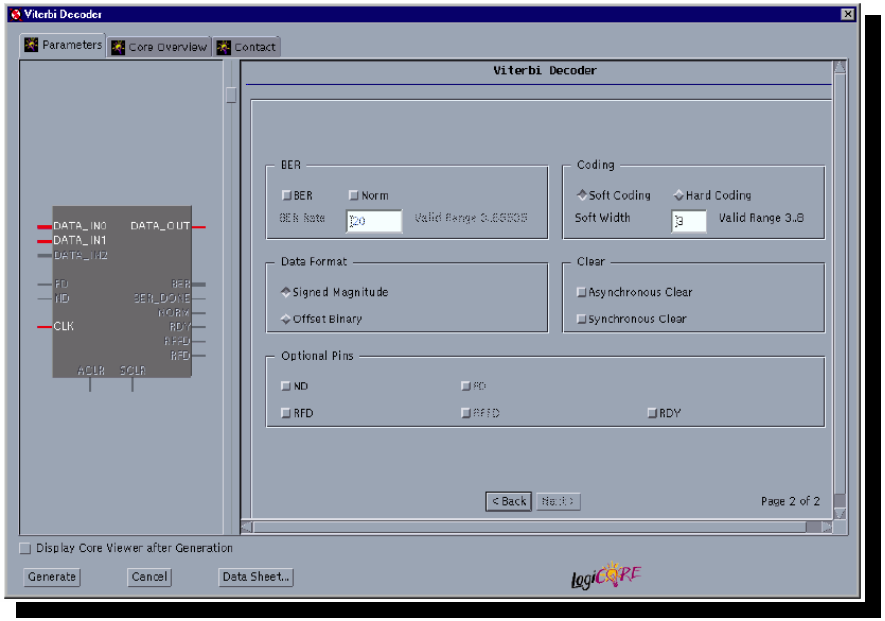
Convolutional Encoder Features

	Output Rate=2	Output Rate = 3	Output Rate = 6	Output Rate=7
Constraint Length	7	7	7	7
Create RPM	Yes	Yes	Yes	Yes
Xilinx Part	XC2V40-6	XC2V40-6	XC2V40-6	XC2V40-6
Area (slices)	7	8	11	12
Maximum Clock Frequency	517MHz	515MHz	505MHz	463MHz

Convolutional Encoder

Xilinx Viterbi Decoder

- General Purpose Parameterizable Netlist
- IEEE802-Compatible Source Code & Netlist
- Parameterizable generator polynomials, puncture rates and constraint lengths
- Built-in BER monitor
- IEEE802-compatible core also supports
  - Best State Calculation for lower latency and improved BER
  - Latency less than 2 microseconds for packet/burst type modems
  - Data rates up to 155Mbps with a single decoder
  - Trellis Coded Modulation
- For more details: http://www.xilinx.com/ipcenter



LogiCORE™ Viterbi

Viterbi Decoder Features

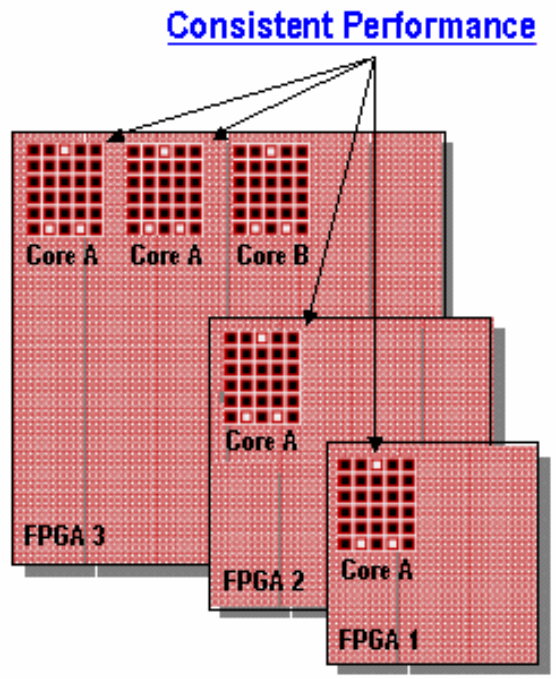
Feature	IEEE 802-Compatible Source Code	IEEE 802-Compatible Fixed Netlist	General Purpose Parameterizable Netlist
Adaptive Code Rates (via erasure inputs)	Yes	Yes	Yes
Adaptive Traceback Depth	Yes	Yes	No
Includes Best State Calculation	Yes	Yes	No
BER Monitor	Yes[1]	Yes[1]	Yes
Latency[2] (MHz)	2µs @ fclk = 157 traceback = 96	2µs @ fclk = 157 traceback = 96	3µs @ fclk = 126 traceback = 96
Parallel/serial Option	No	No	Yes
Constraint Length (k)	K = 7	K = 7	Parameterizable (3 to 9)
Generator Polynomials	G0=171, G1=133; or G0=133, G1=171	G0=171, G1=133; or G0=133, G1=171	Parameterizable
Decoder Rate	1/2	1/2	Parameterizable (1/2 to 1/7)
Dual Rate	No	No	Parameterizable rates & codes, selectable via select pins

Feature	IEEE 802-Compatible Source Code	IEEE 802-Compatible Fixed Netlist	General Purpose Parameterizable Netlist
Trellis Code Modulation Support	Yes[3]	Yes[3]	No
Internal Puncturing Option	No	No	Fixed rate, selectable from 2/3 to 12/13. Parameterizable puncture codes.
Simulation Support	VHDL Source	Gate Level	VHDL Behavioral Model
Proposed Applications	IEEE 802.11a/16a-compatible fixed wireless applications such as LMDS and MMDS. Also HiperLAN2, DVB, and OC3 data rates.	IEEE 802.11a/16a-compatible fixed wireless applications such as LMDS and MMDS. Also HiperLAN2, DVB, and OC3 data rates.	General purpose (Any - DVB, 3GPP, etc.)
Format	Source Code (Parameterizable)	Fixed Netlist	Parameterizable Netlist using the CORE Generator System
Supported Devices	Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Spartan-II, Spartan-IIE	Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Spartan-II, Spartan-IIE	Virtex, Virtex-E, Virtex-II, Virtex-Pro, Spartan-II, Spartan-IIE

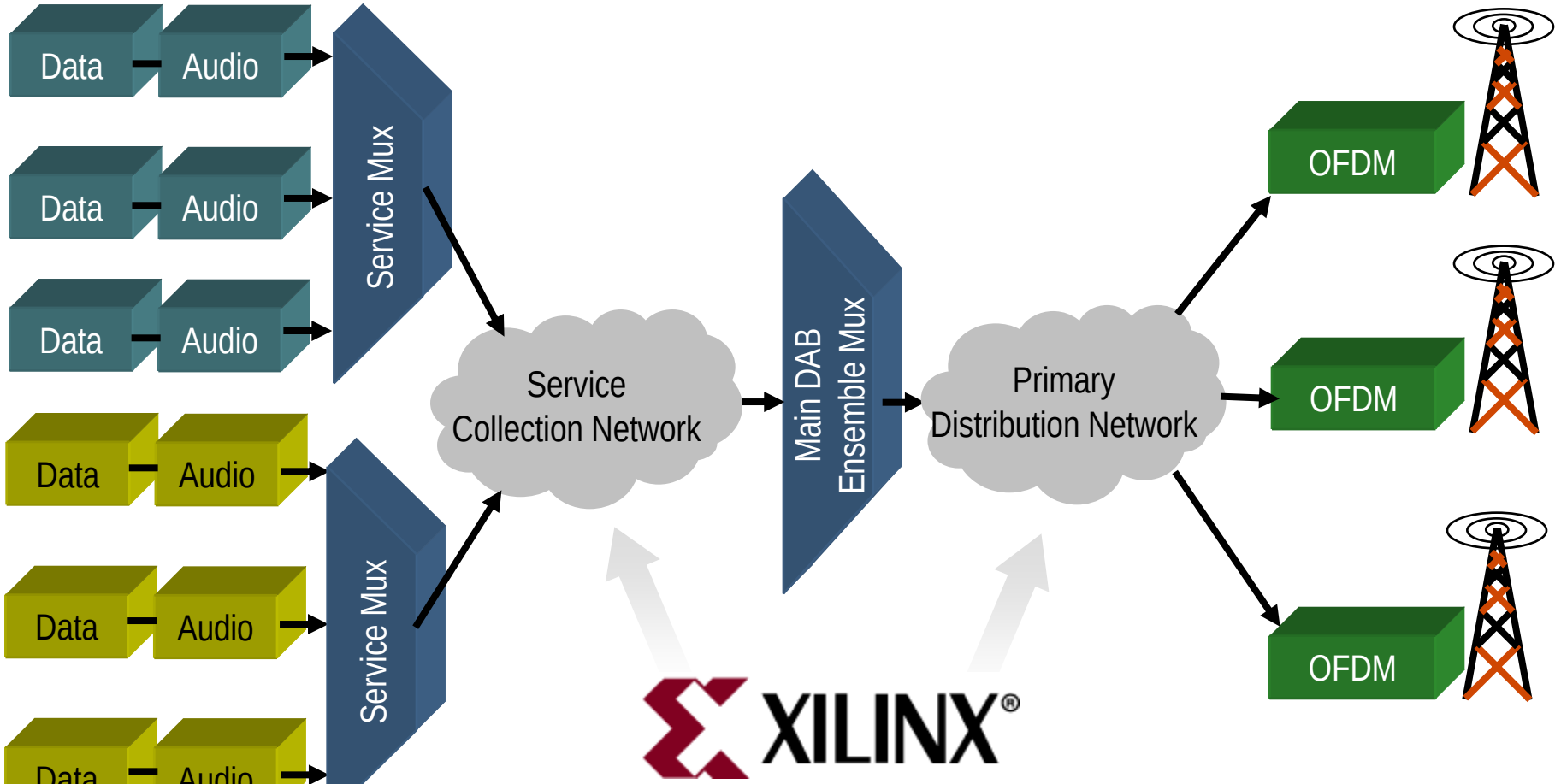
Viterbi

Smart-IP Technology

- Used in all Xilinx cores
- Results in predictable implementation
  - Consistent functionality and performance
  - Independent of core placement, number of cores used, surrounding user logic, device size and choice of EDA tool
- Vital for easy design of multi-channel systems



Single Frequency Networks

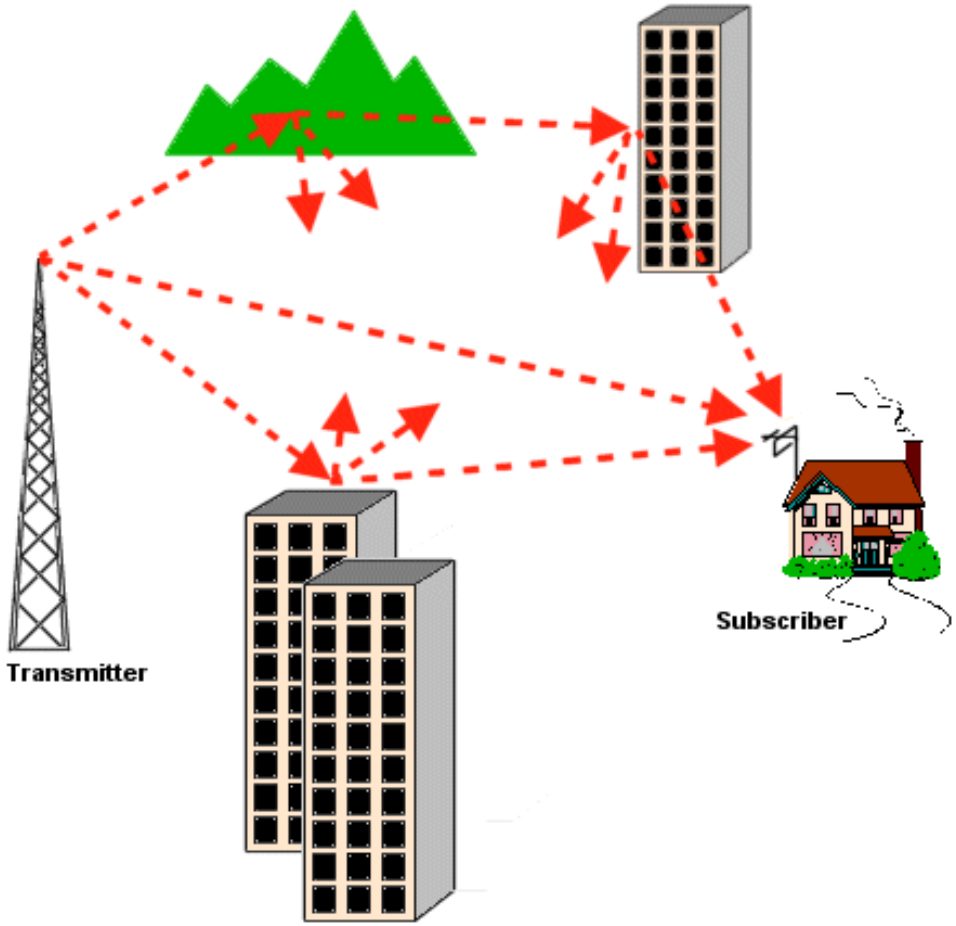


FPGAs widely used in WAN/MAN applications

See xilinx.com/esp/optical for more details

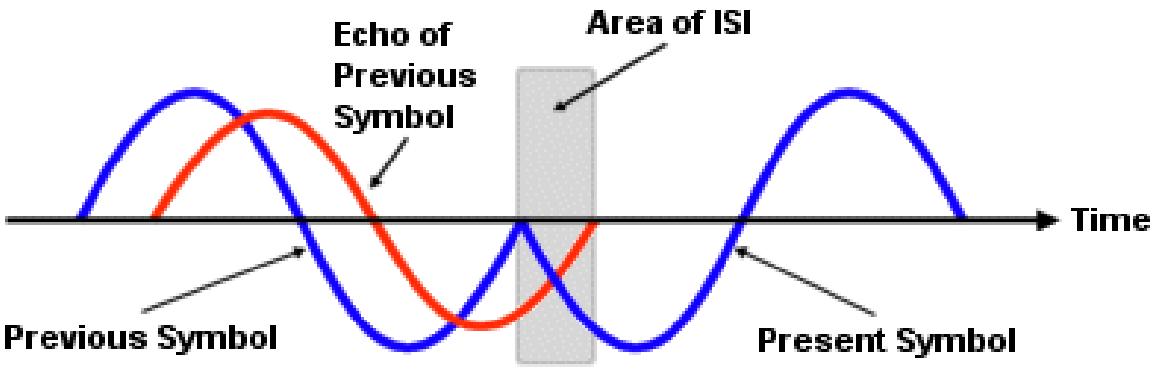
Multipath Signals

- Multipath or reflected signals can cause interference
- Can add constructively or destructively to main (shortest) path
- Reflections are delayed and can cause ISI *(next slide)*
- DVB/DAB solution is to use Coded Orthogonal Frequency Division Multiplex (COFDM)



Inter-Symbol Interference (ISI)

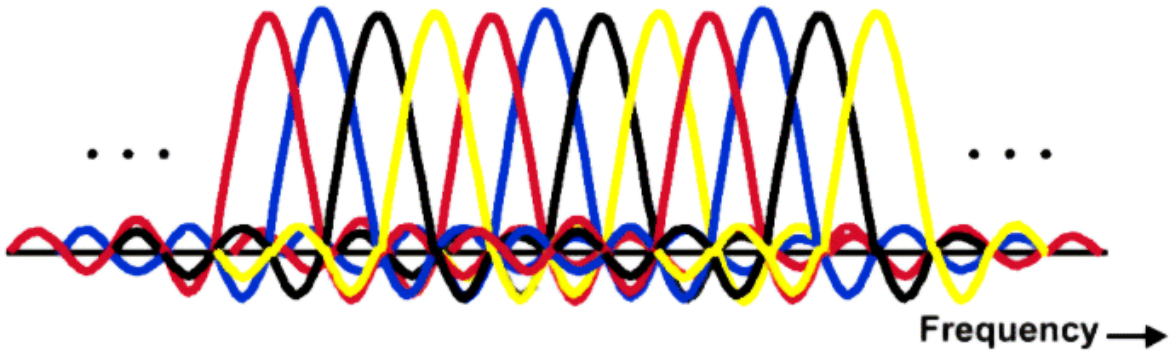
- An echo of the previously received symbol can interfere with present symbol reception



- Area of ISI is also called delay spread and for transmission to work effectively, this must be removed
- Removal is done using a number of steps…..

Frequency Division Multiplexing

- FDM is a way of increasing the symbol period so that the delay spread is only a small fraction of it
- A single high frequency carrier is divided into many lower frequency parallel carriers : up to 6817 in DVB systems



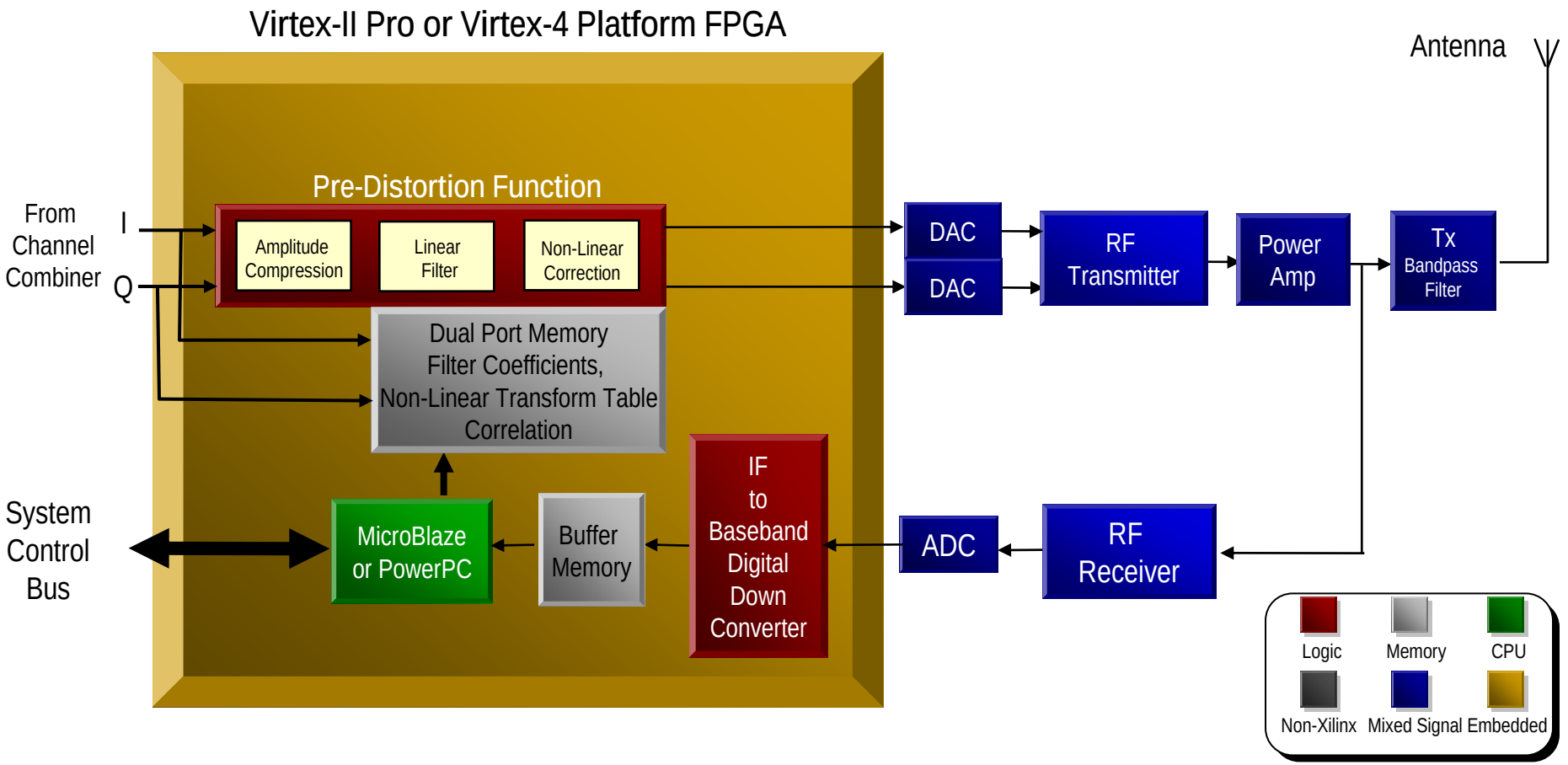
- The carriers are orthogonal to one another - they are spaced $1/T_u$ apart where T_u is the symbol period
- FDM is implemented using an Inverse Fast Fourier Transform (IFFT) at the transmitter and a Forward FFT at the receiver

Baseband Shaping in FPGA

- Before transmission, signals are shaped using a filter such as the *Root Raised Cosine* (RRC) filter
- Maximises the use of total available bandwidth whilst also eliminating *intersymbol interference* (ISI)
- RRC coefficients determined using DSP tools (e.g. Matlab)
  - Designer enters required roll-off and bit rate parameters into RRC generator to produce coefficients
  - Suggests number of taps and shows resulting waveforms for trial and error iterations
- Final RRC coefficients simply entered into Xilinx Core Generator to build necessary FIR filter in hardware

Xilinx Pre-Distortion System

Using a Processor For Coefficient Calculation & Tracking

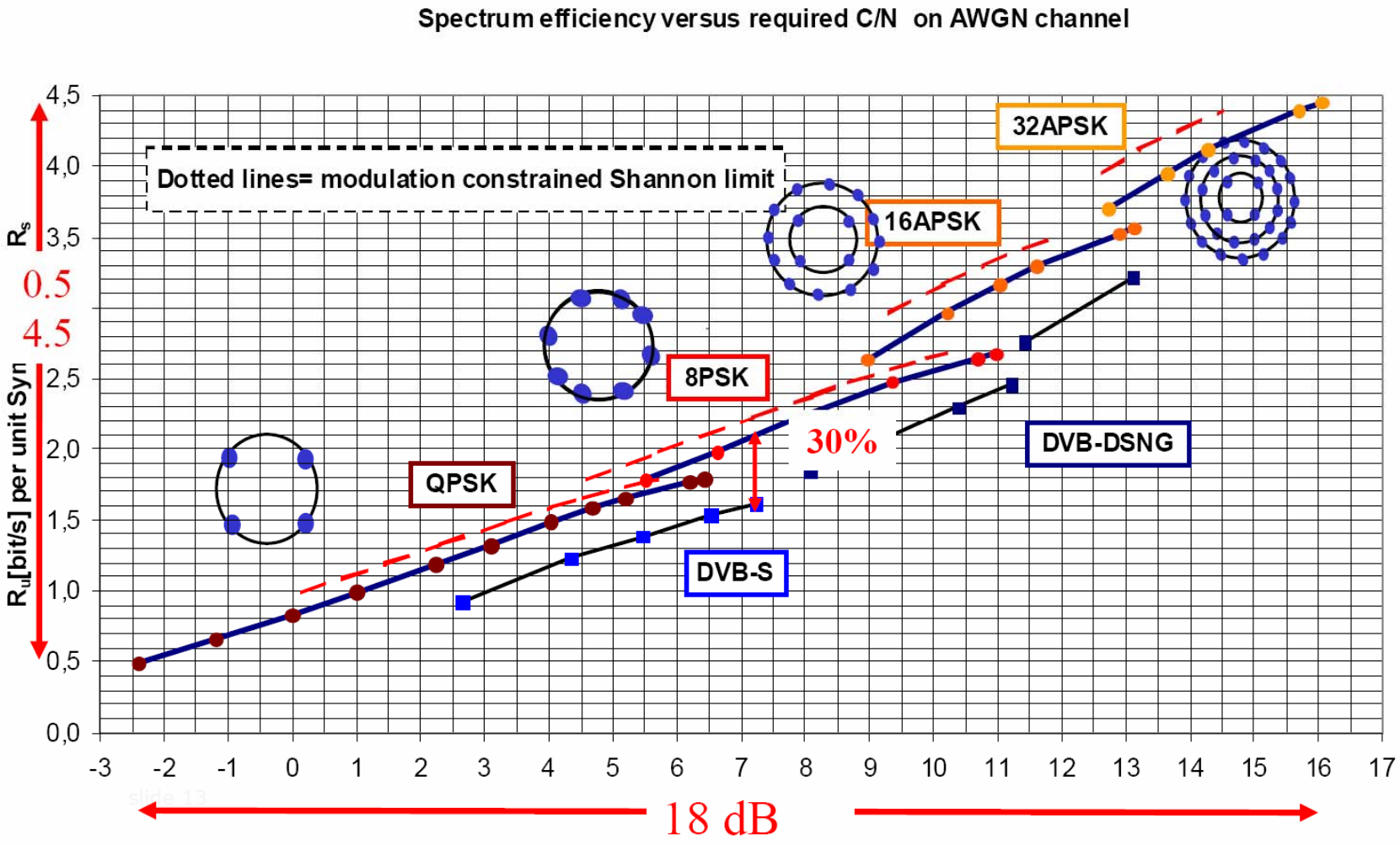


DVB-S2

Second Generation Broadband Satellite Standard

- Increased system capacity over DVB-S
  - Up to 40% better satellite transponder utilization in broadcast mode
  - Up to 200% more subscribers per unit of bandwidth in interactive mode
  - Still backward compatible with DVB-S
- Improved link margin
  - Increased availability, extended coverage and enhanced robustness to noise and interference
- Flexibility to match a wide range of transponder characteristics
- Multiple input formats supported :
  - MPEG-2, MPEG-4 and HDTV transport streams
  - Generic streams of IP packets and ATM cells
- Multiple transport streams in a single modulated carrier
- Adaptive coding and modulation

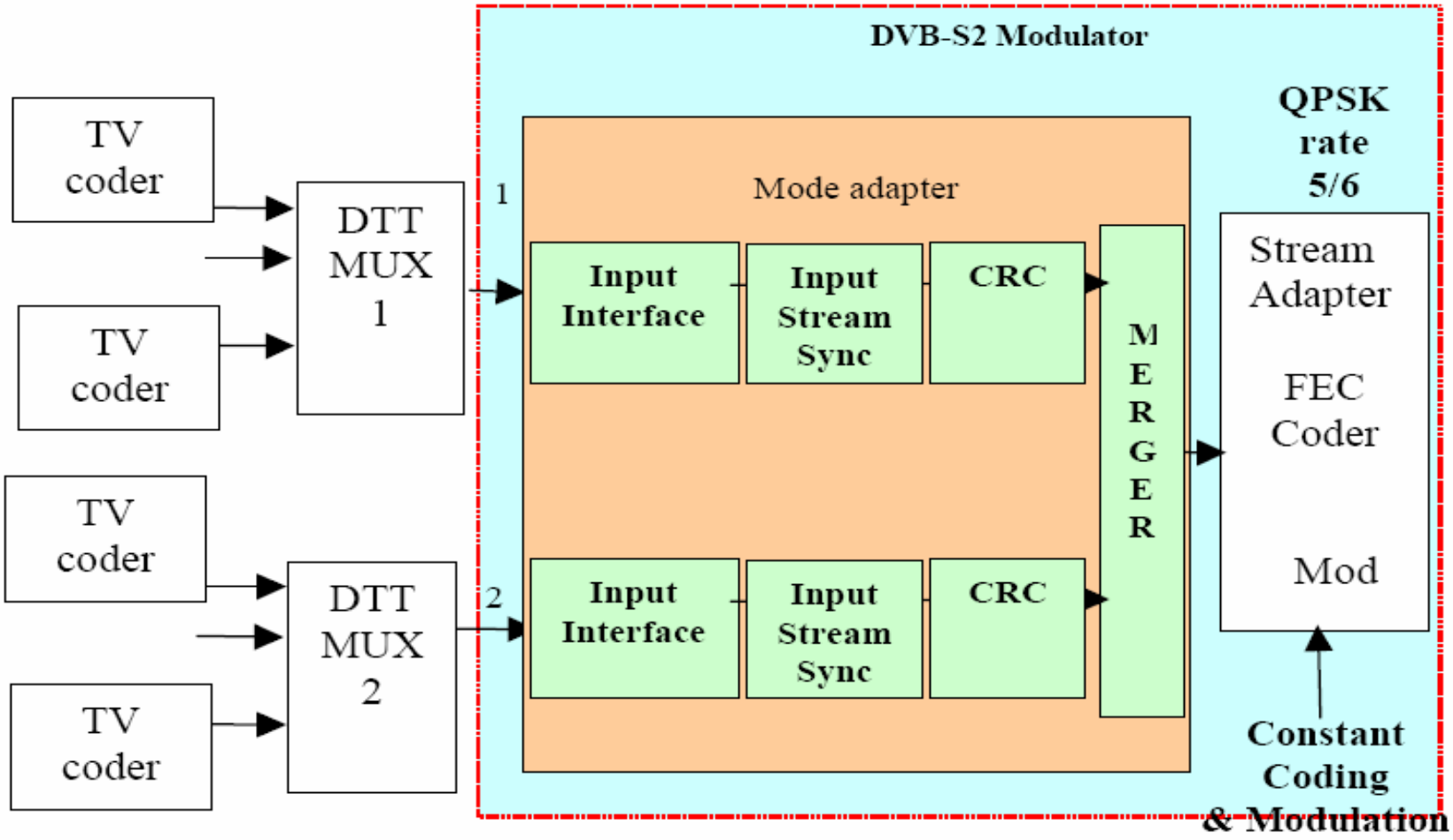
DVB-S2 Nearer Shannon Limits



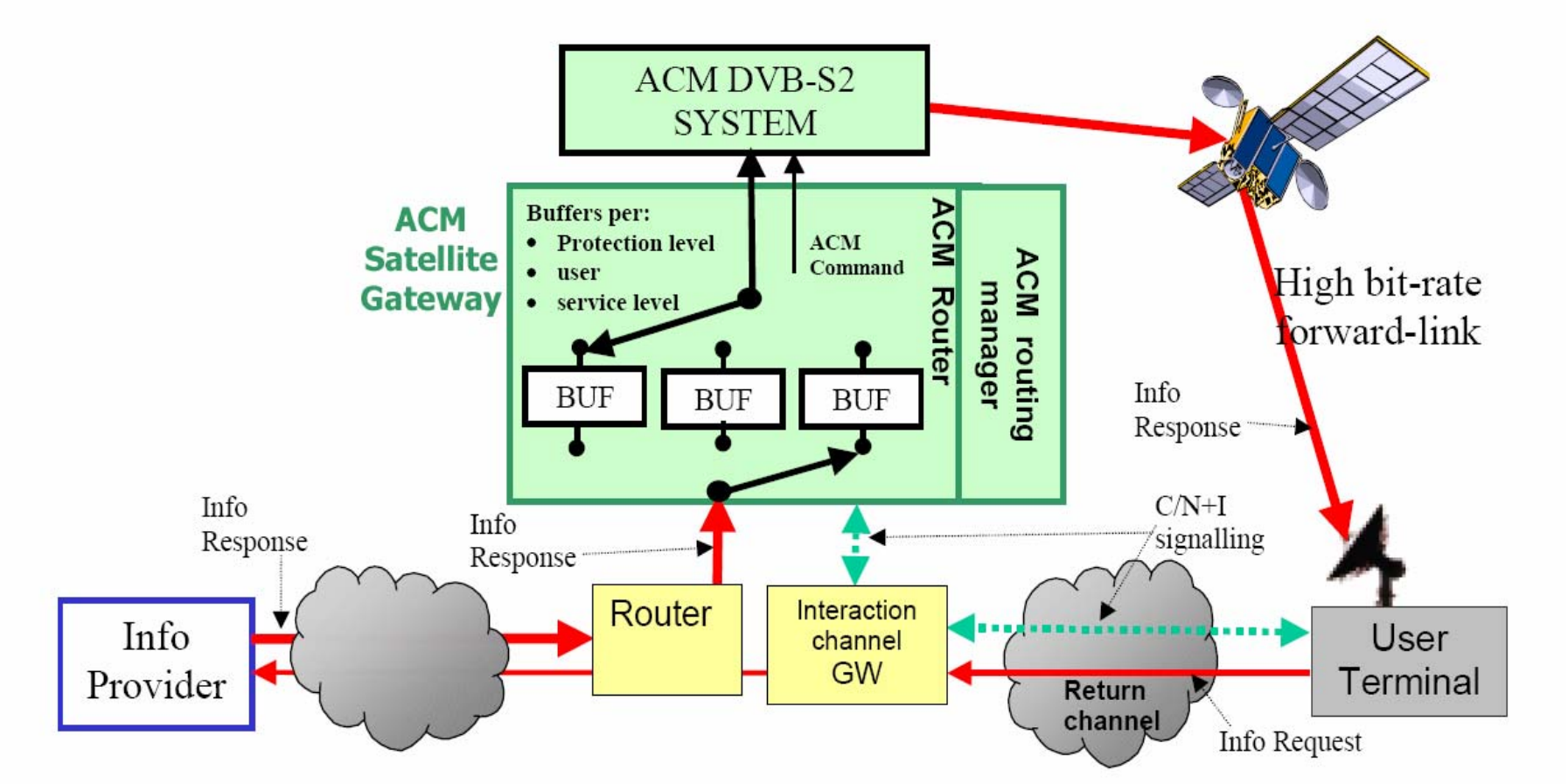
DVB-S2 vs. DVB-S Example

Satellite EIRP (dBW)	51	
System	DVB-S	DVB-S2
Symbol-rate MBaud	27.5 (α=0.35)	30.9 (α=0.20)
Modulation & coding (C/N=5.1dB@27.5 MHz)	QPSK 2/3	QPSK 3/4
Useful bit-rate Mbit/s	33.8	46 (gain 39%)
Number of SDTV programmes (*)	7 MPEG-2; 15 AVC	10 MPEG-2 21 AVC
Number of HDTV programmes (*)	1-2 MPEG-2; 3-4 AVC	2 MPEG-2 5 AVC

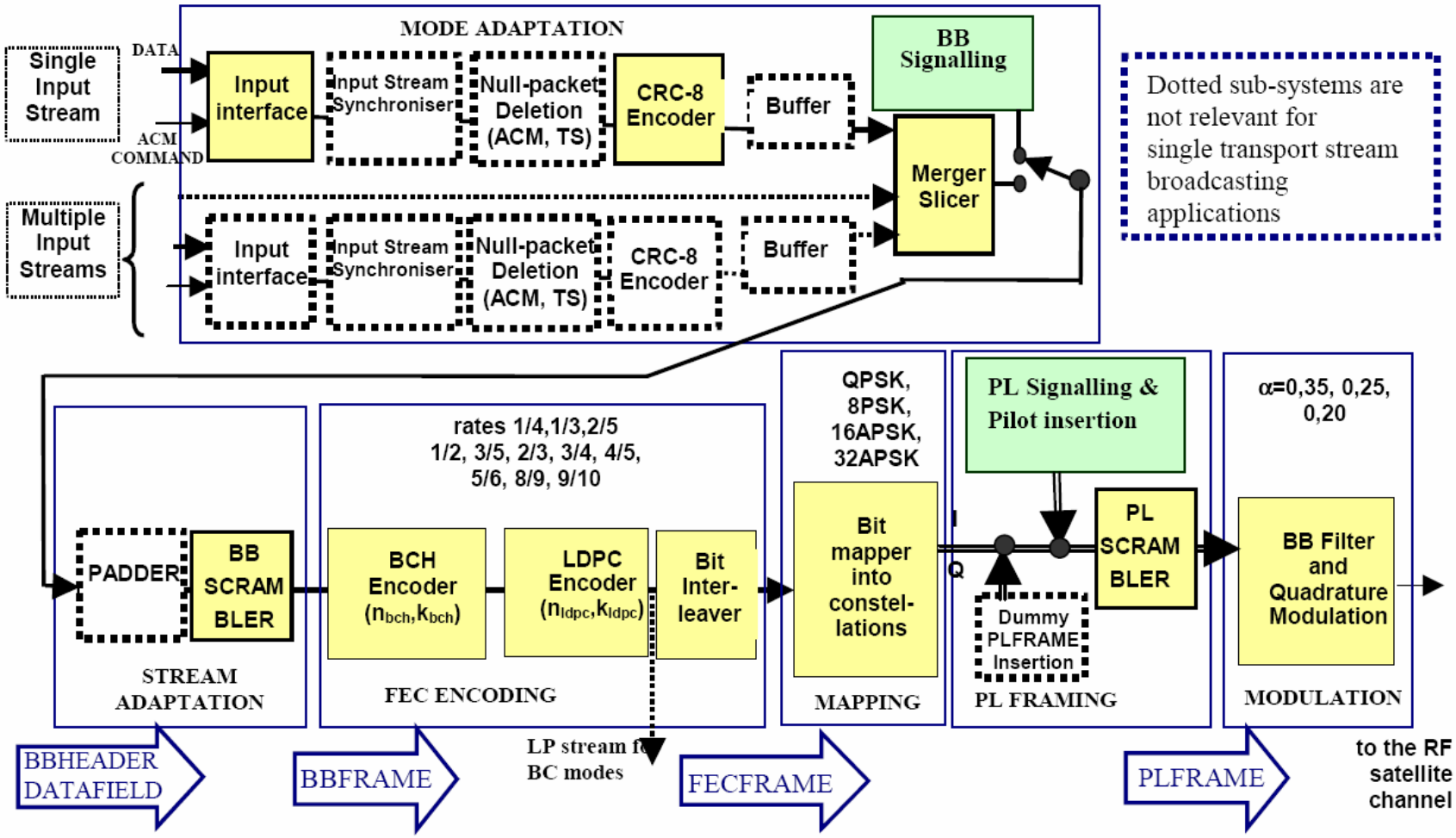
Multiple Muxes to DTT Tx



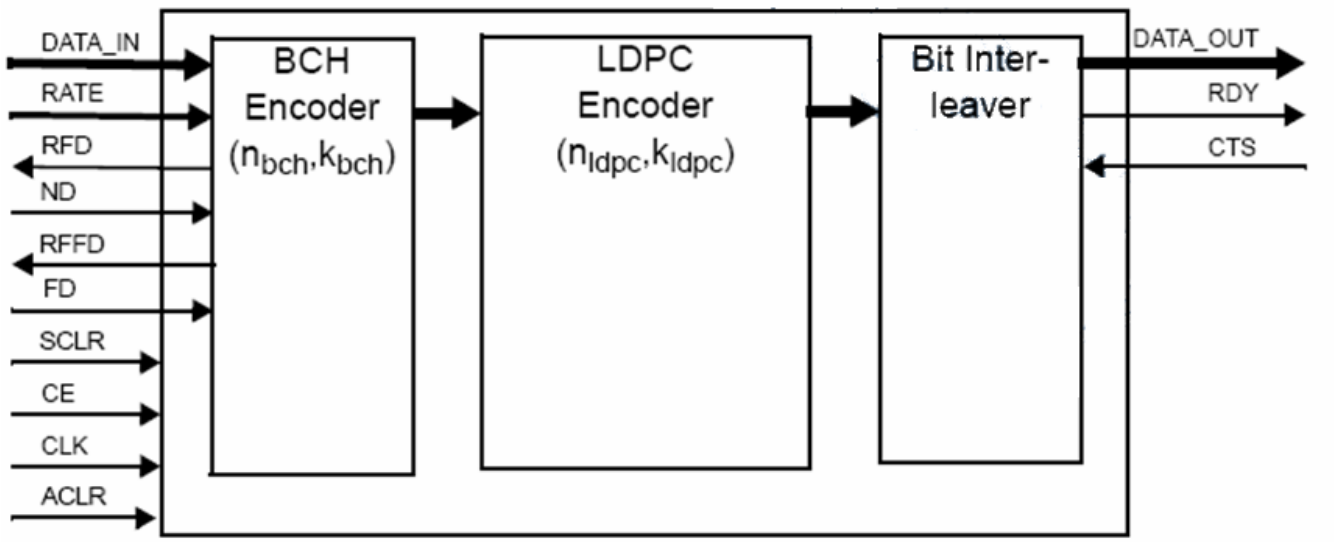
IP Services over DVB-S2



DVB-S2 Standard

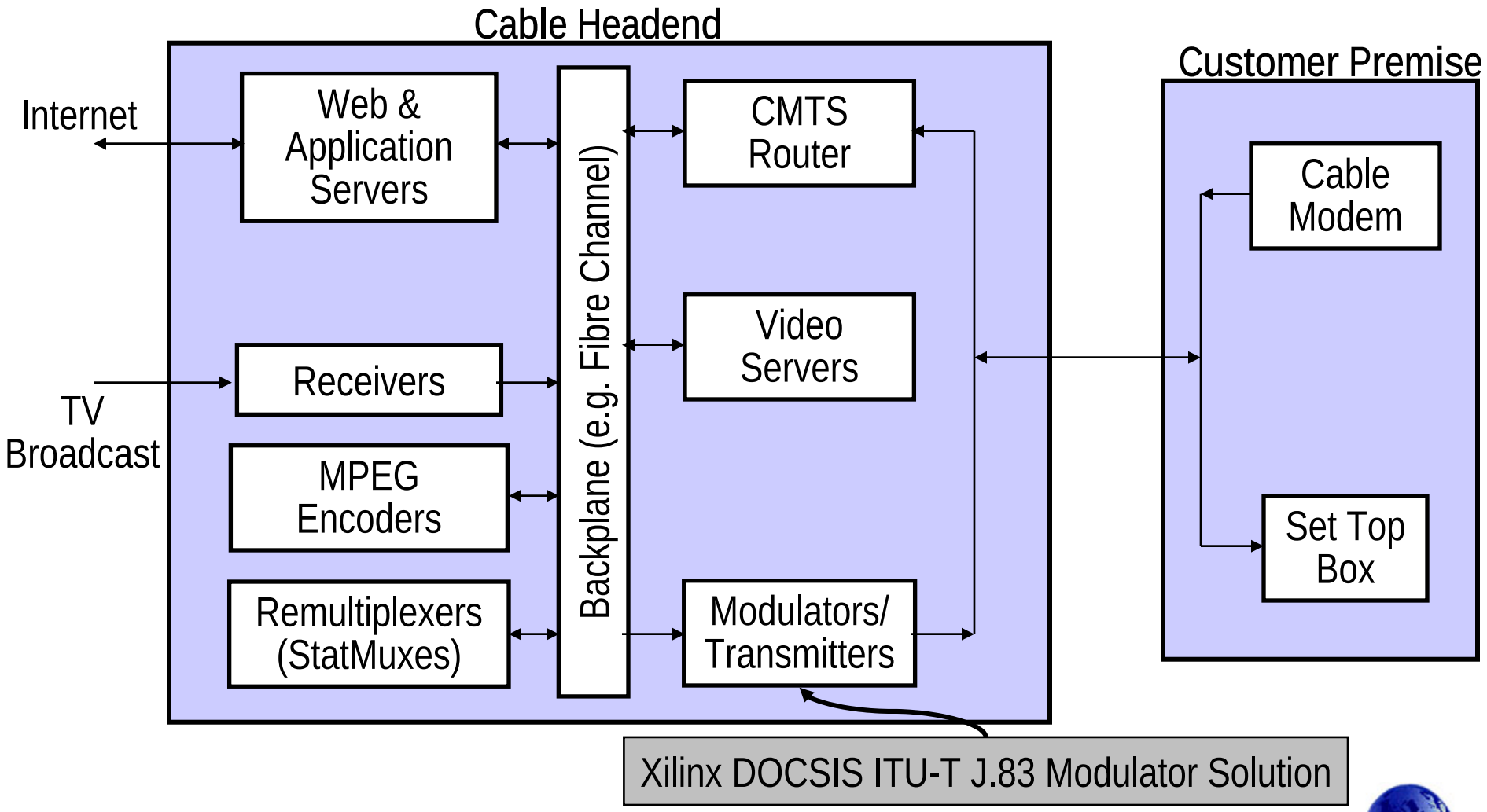


Xilinx DVB-S2 FEC Solution



Width (W)	Slices	Block RAM	MULT 18x18	Max. Clock Frequency (MHz)			Maximum Encoded Output Rate bits/s		
				-7	-6	-5	-7	-6	-5
1	430	19	1	230	200	170	230	200	170
2	600	19	2	230	200	170	460	400	340

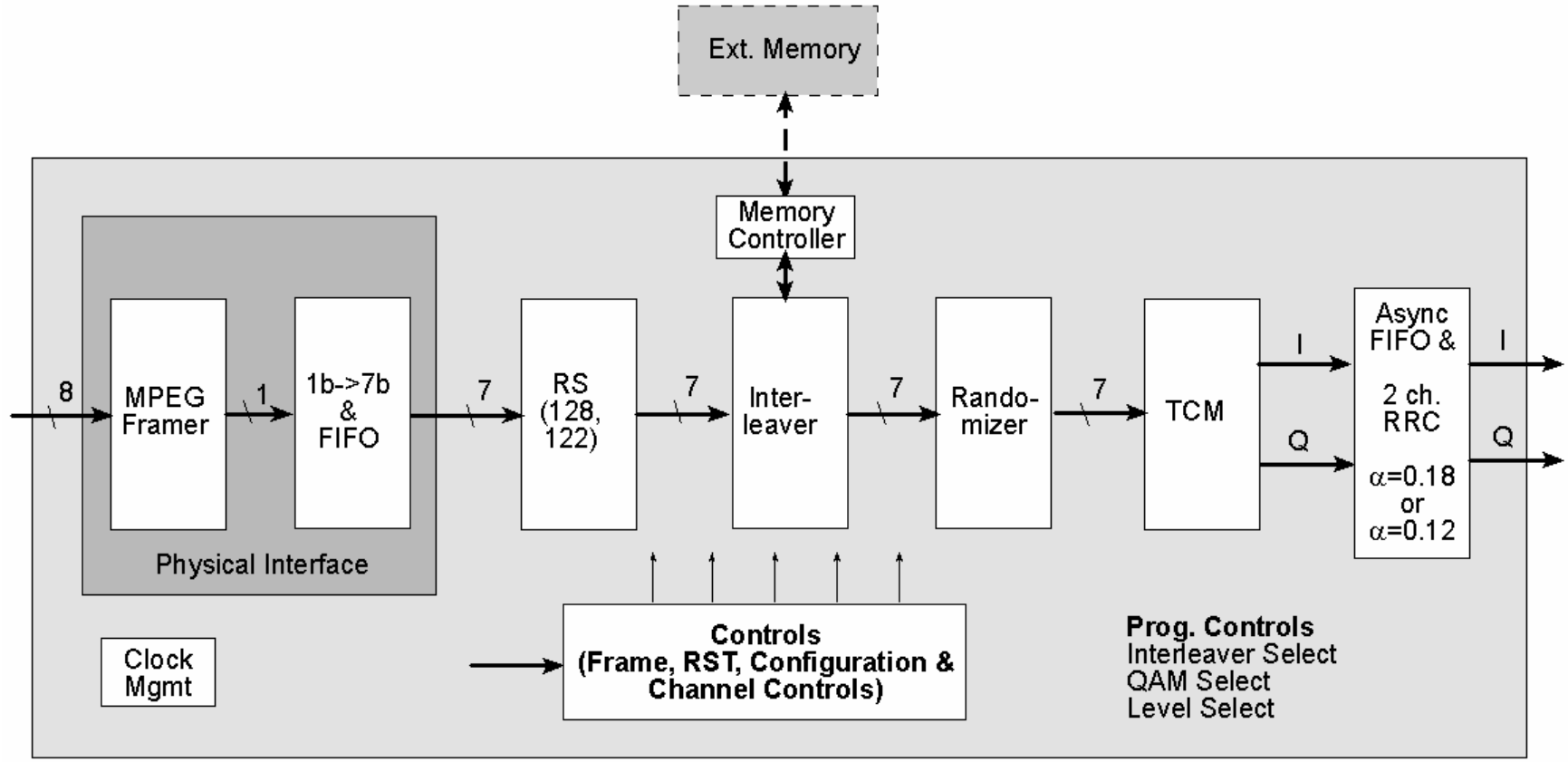
J.83 in the Broadcast Chain



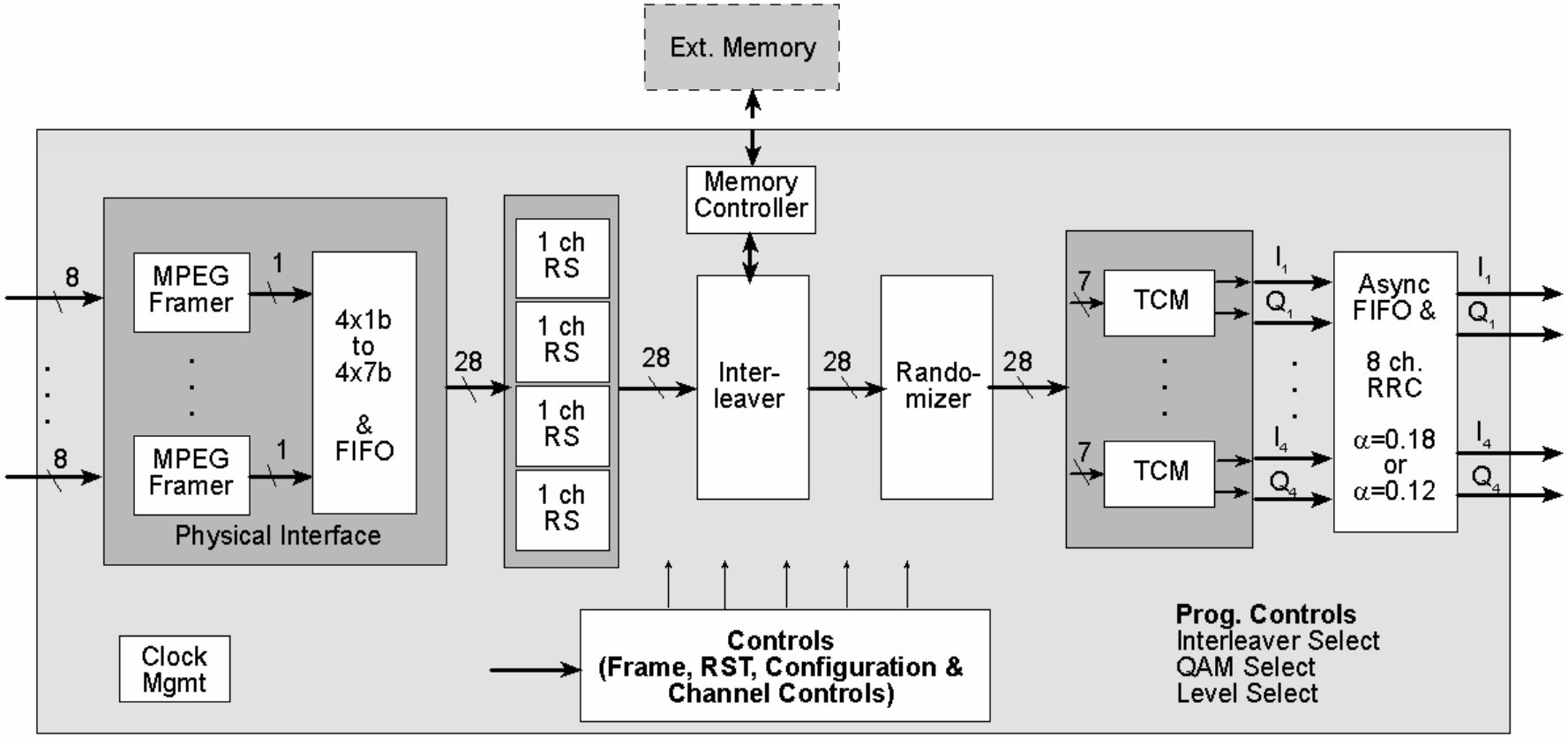
J.83 Annex A/B/C Modulators

- J.83 Annex A/C, DVB-C, DVB-MC(EN 300 749), DAVIC, IEEE 802.14 compliant
- Designs may be used in one of two footprints
  - Single Channel :group of 1
  - Four Channel : group of 4
- Multi-channel designs may be constructed out of either granularity

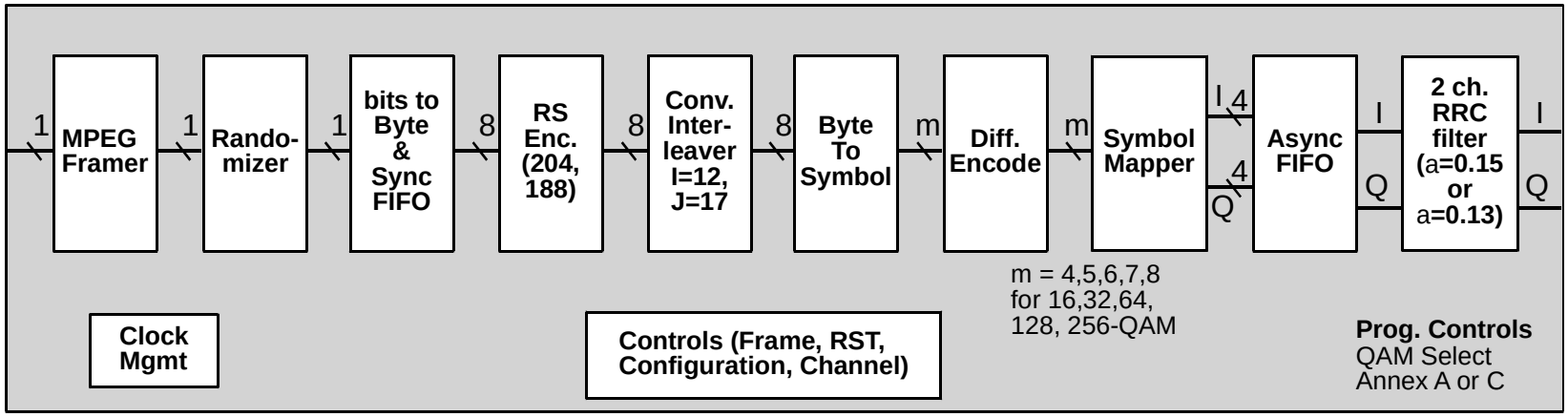
Single Channel J.83 Annex B Modulator



Four Channel J.83 Annex B Modulator

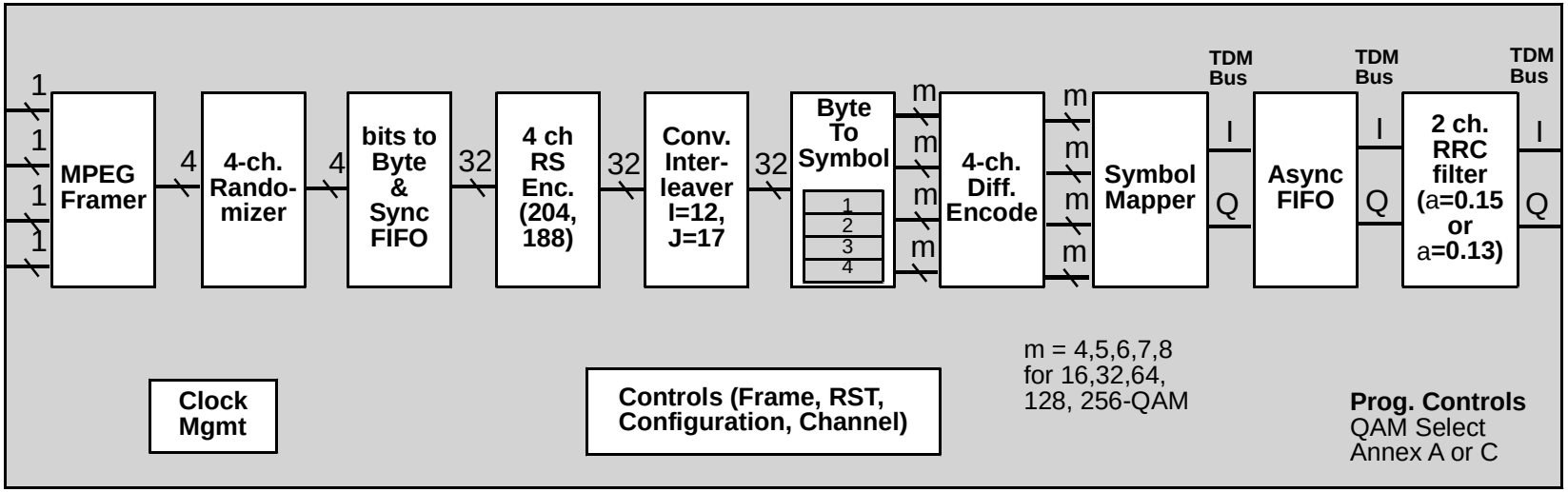


Single Channel J.83 Annex A/C Modulator



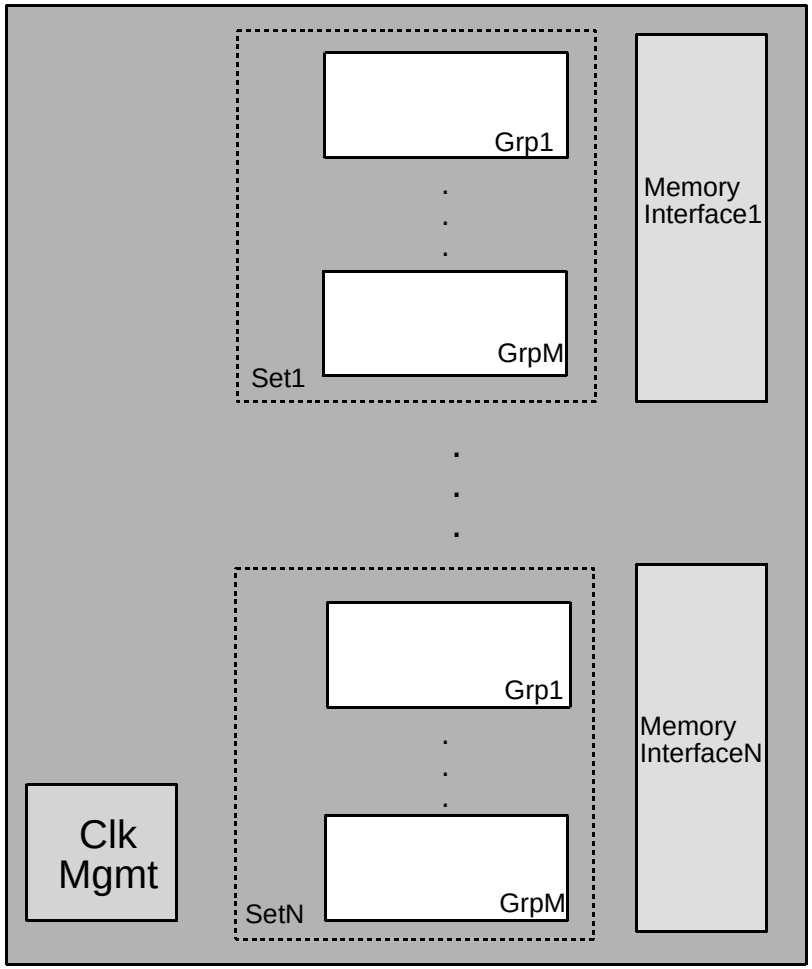
Single Channel Granularity of a Group

Four Channel J.83 Annex A/C Modulator



Four Channel Granularity of a Group

Multi-Channel Design



- 1 Group = 1 or 4 channels
- M = #groups per memory
- N = #channels/#memory
- M,N dependent on the max clock speed of the memory and design clock speed.

Additional J.83 Info

- Multi-channel Design
  - Granularity of 1 or 4 channels
  - Common Control Parameters for 4 channel granularity
    - Runtime QAM Selection(64 or 256)
    - Runtime Interleaver Switching (16 possible cases)
- Interface to External Memory for Interleaver
  - ZBT SRAM(Micron's ZBT SRAM based controls signals)
  - 7(28) bits memory width for granularity of 1(4)
- Clock Management Scheme included
  - Soft as well as Hard Reset for the design
  - Separate Soft reset for each group
  - Single Hard reset for the design
- Optional RRC Filter provided
- Design Source is in combination of sysgen files(.mdl,.m) plus vhdl and .edn
- Design will be delivered as set of vhdl and .edn files

Xilinx DOCSIS J.83 A/B/C

Key Features & Benefits

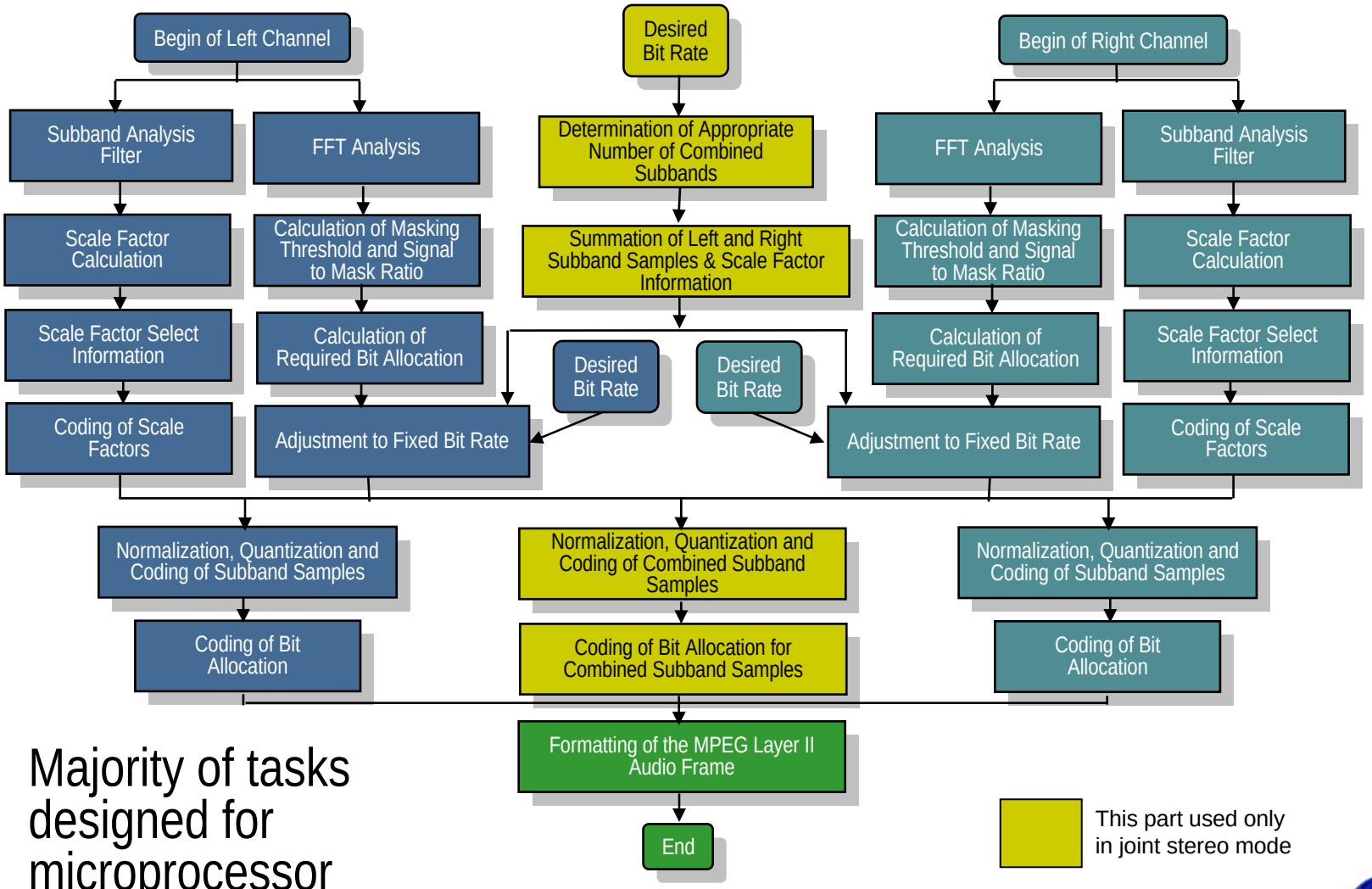
- Unprecedented levels of integration, driving down the cost per channel
- Variable input symbol rates, providing support for multiple types of input streams such as MPEG-2 or ATM packets
- Single and multi-channel solutions, delivering the optimal integration and flexibility for multi-channel designs in a Virtex-II Pro
  - Multi-channel design leverages unique Xilinx silicon features such as the SRL16, resulting in compact implementation
- Programmable 64 and 256 QAM modulation, conforming to the J.83 Annex B specification
- Variable interleaver and parameterized RRC filter as defined in the J.83 Annex B specification
- Common controls for multi-channel design, providing efficient resource sharing
- Supported in the popular System Generator for DSP software platform design
- Less than $3* per channel in a Spartan-3, providing an extremely low cost solution
- Learn more at http://www.xilinx.com/ipcenter/j83_mod/index.htm

Xilinx DOCSIS J.83 A/B/C

More Key Features & Benefits

- Higher Flexibility
  - Designers don't always want entire solution (differentiate)
  - ASSP limits what the customer can do
  - FPGA enables the designer to create a customized solution around the Xilinx Modulator
    - Customer gets System Generator for DSP model
    - Fully Parameterizable
- Lower Cost
  - Lower price per channel
  - We believe Xilinx to be lower by at least a factor of 2

DAB MPEG Encoder Flow Chart

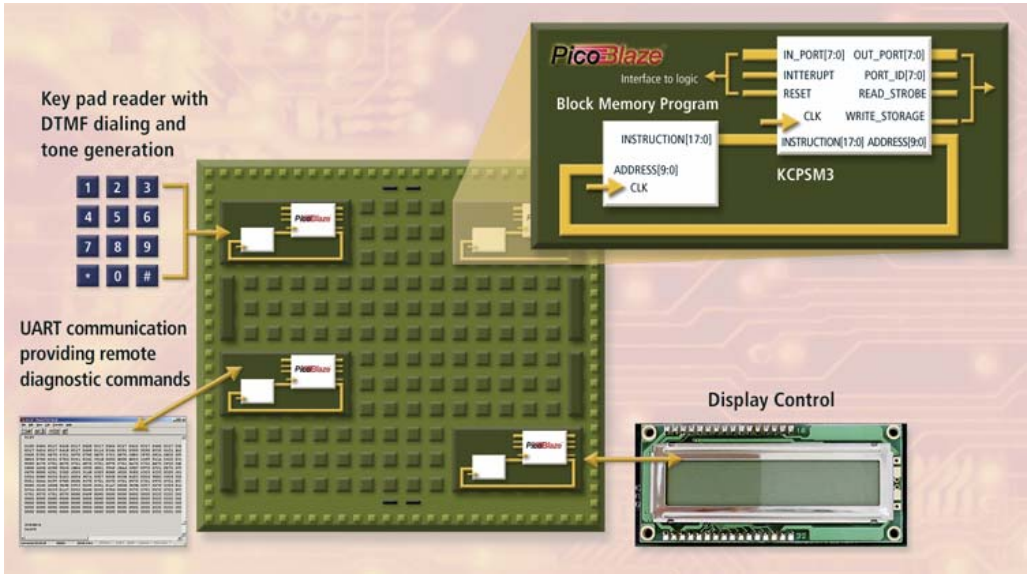


- Majority of tasks designed for microprocessor

Flexible Embedded Processing

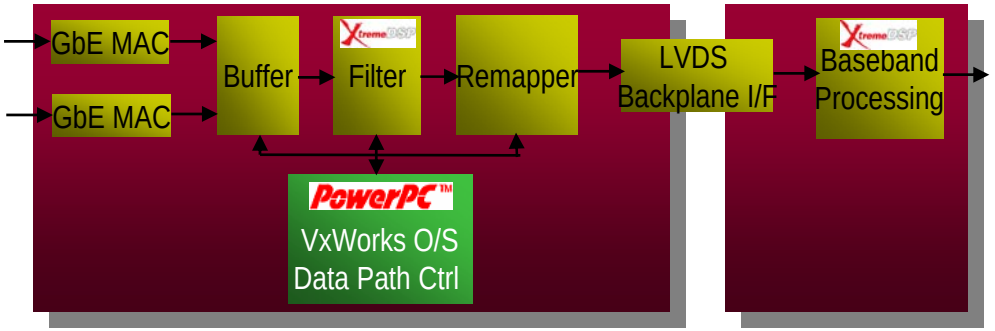
PicoBlaze™

- 8-bit Microcontroller
- Simple state-machines and “localised” on-chip control
- Pixel processing & display control

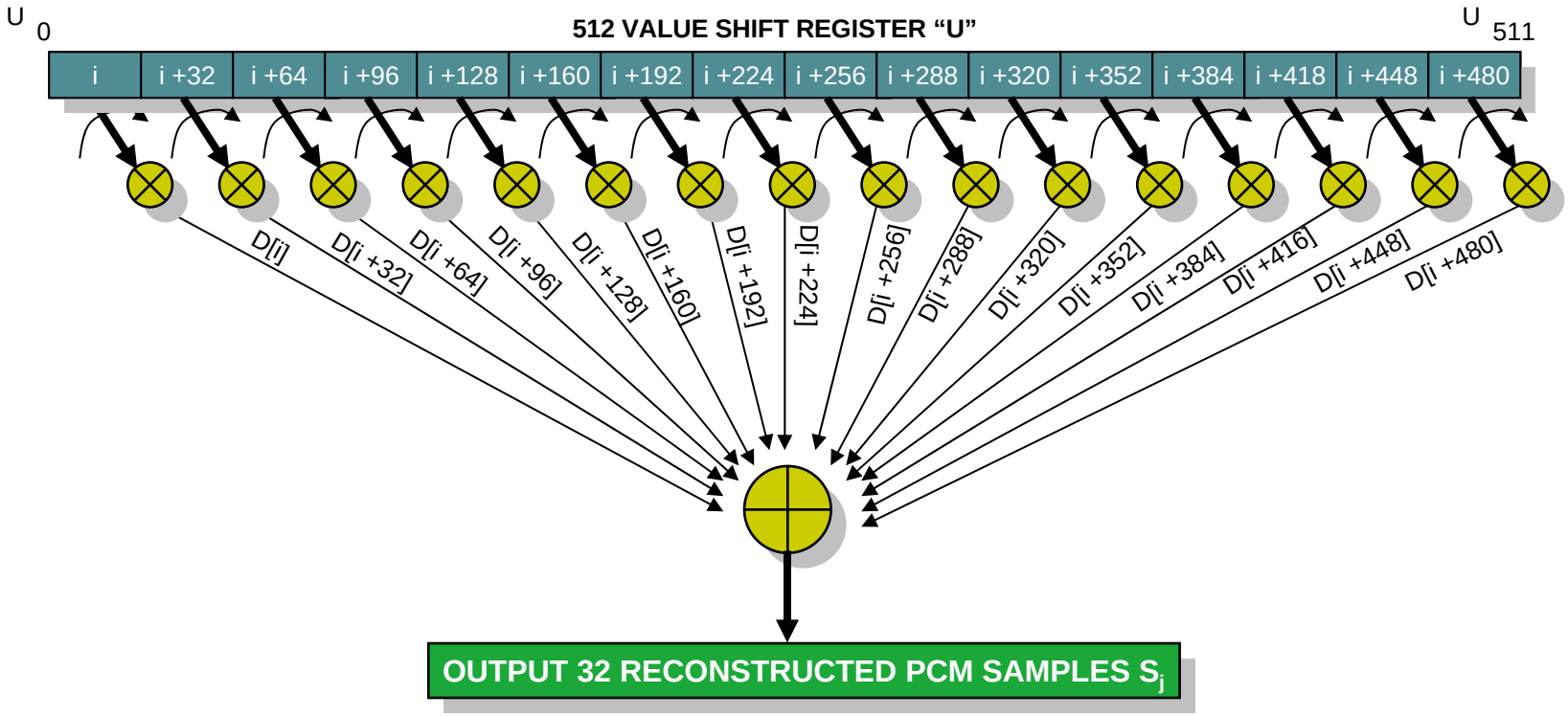


MicroBlaze PowerPC™

- 32-bit Microprocessors
- Cost/performance tradeoffs
- Extensive peripherals, RTOS & bus structures
- Networking & wireless comms, control & instrumentation



MPEG Synthesis Subband Filter



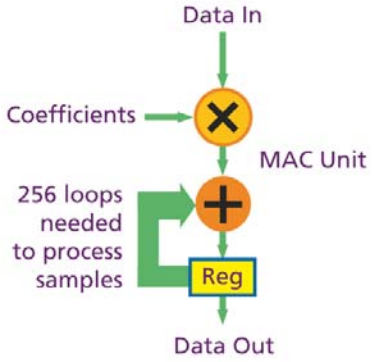
- Well suited to parallel FPGA structure
- Increased performance from dedicated hardware co-processing
- Support parallel DAB frame processing on one device

Why FPGAs for Transmission?

High Computational Workloads

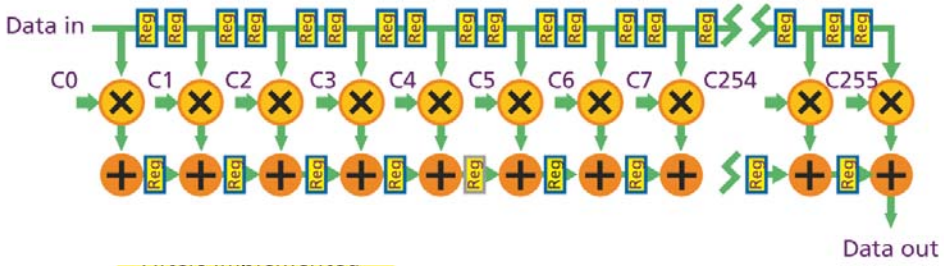
256-tap Filter Example

Conventional DSP Processor - Serial



$$\frac{1\ \text{GHz}}{256\ \text{clock cycles}} = 4\ \text{MSPS}$$

FPGA-based DSP - Parallelism

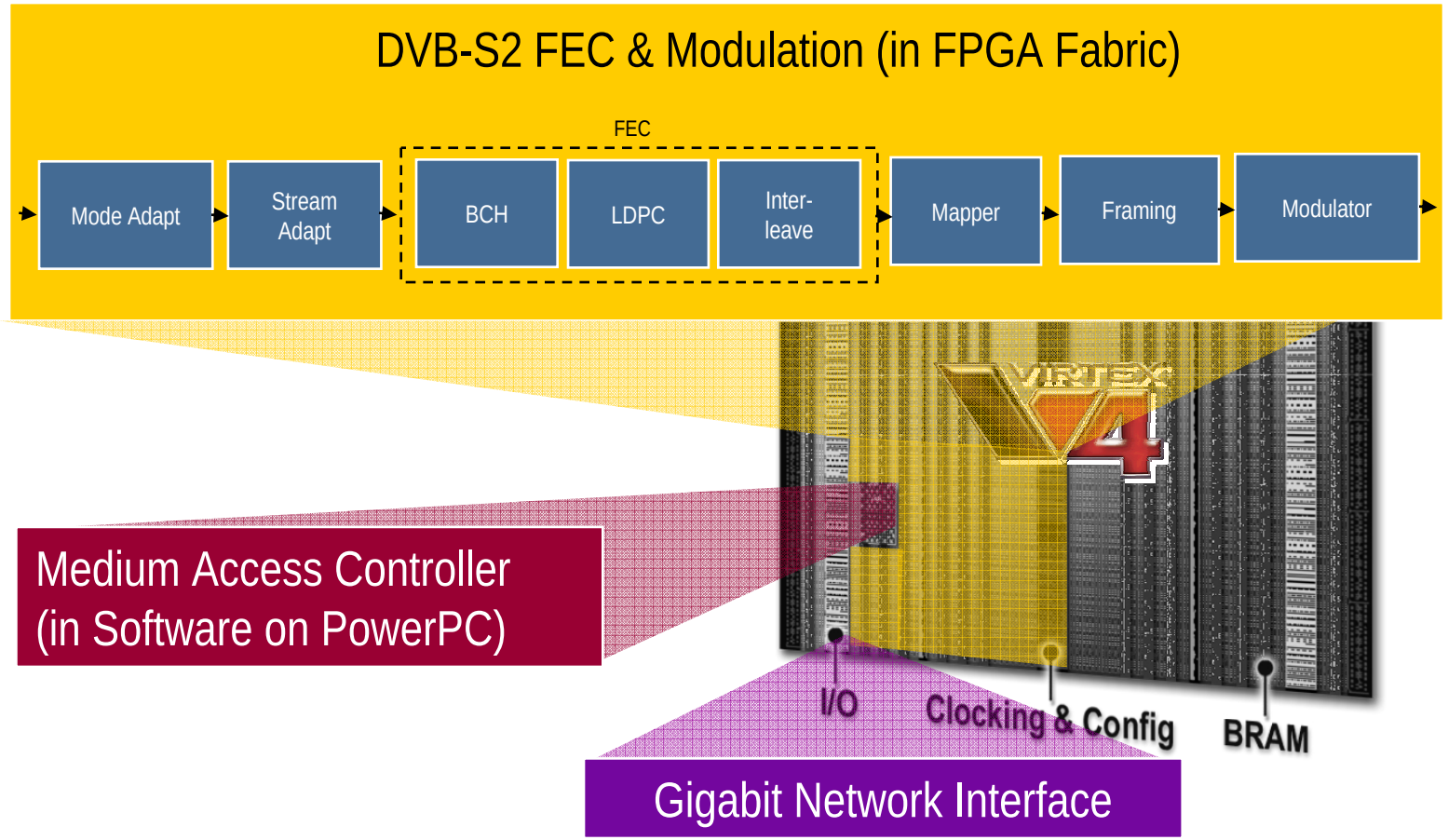


$$\frac{500\ \text{MHz}}{1\ \text{clock cycle}} = 500\ \text{MSPS}$$

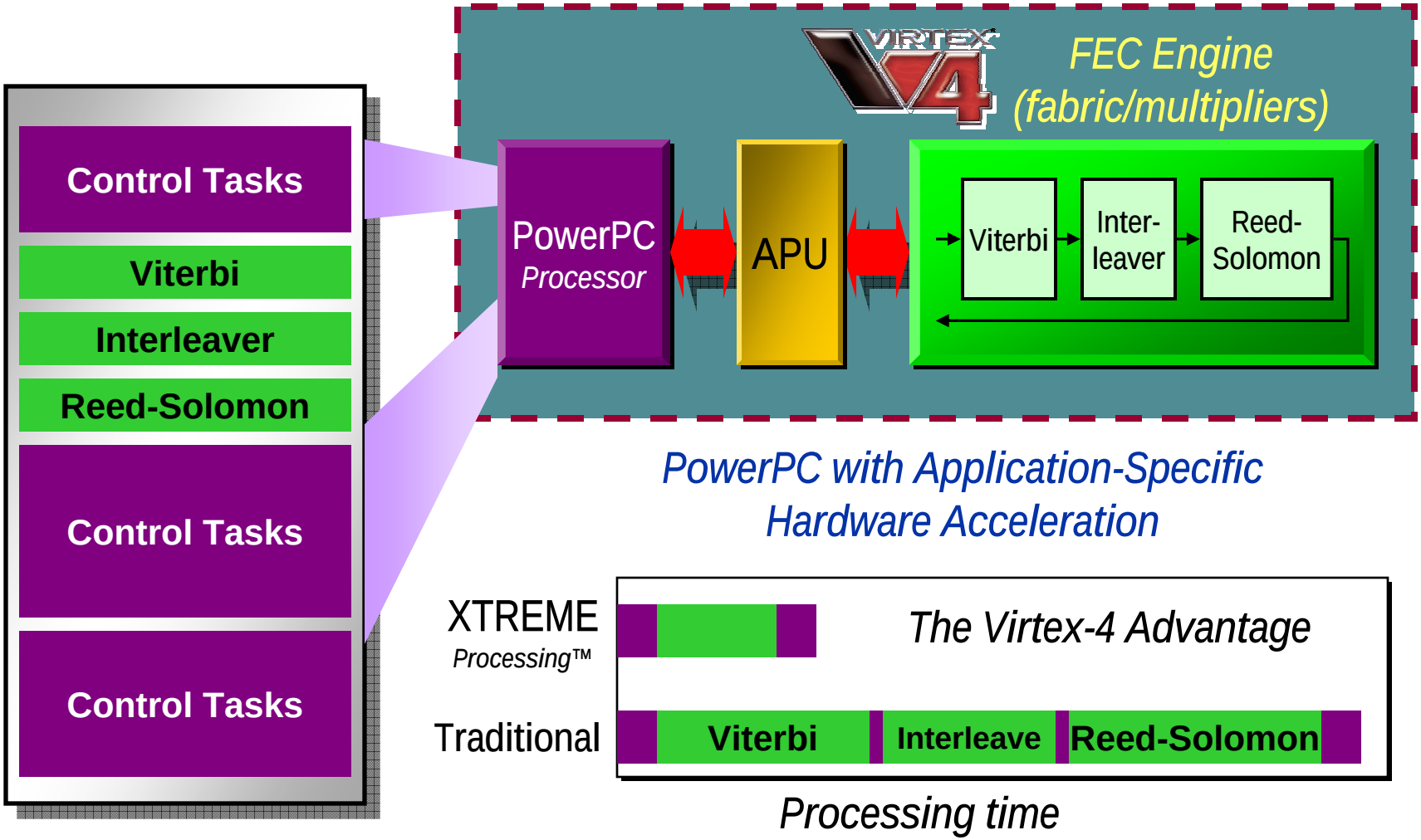
Virtex-4 FPGAs Enable New Development Paradigm

- Ability to run hardware and software in-situ at speed, with real-time observability & debug
- Ability to provide dedicated hardware to all software developers early and at low cost
- Ability to adjust hardware/software tradeoff
  - *During definition*
  - *During debug*
  - *After shipment*

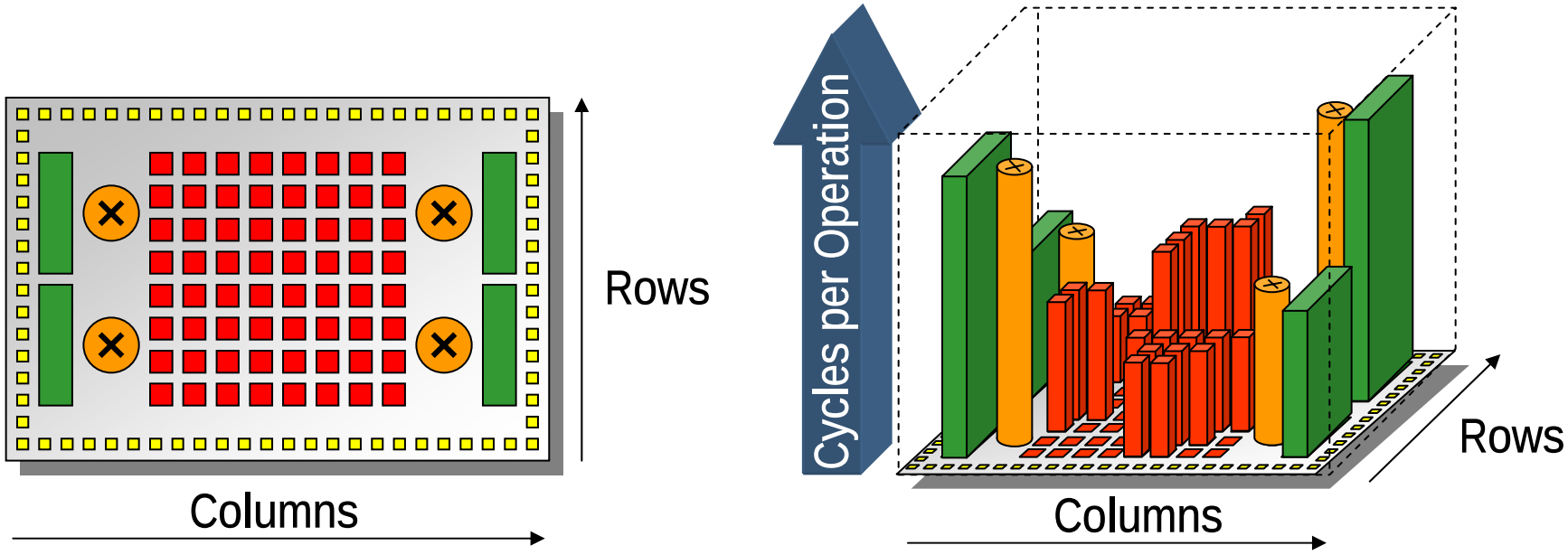
HW/SW Partition Example



Xtreme Forward Error Correction



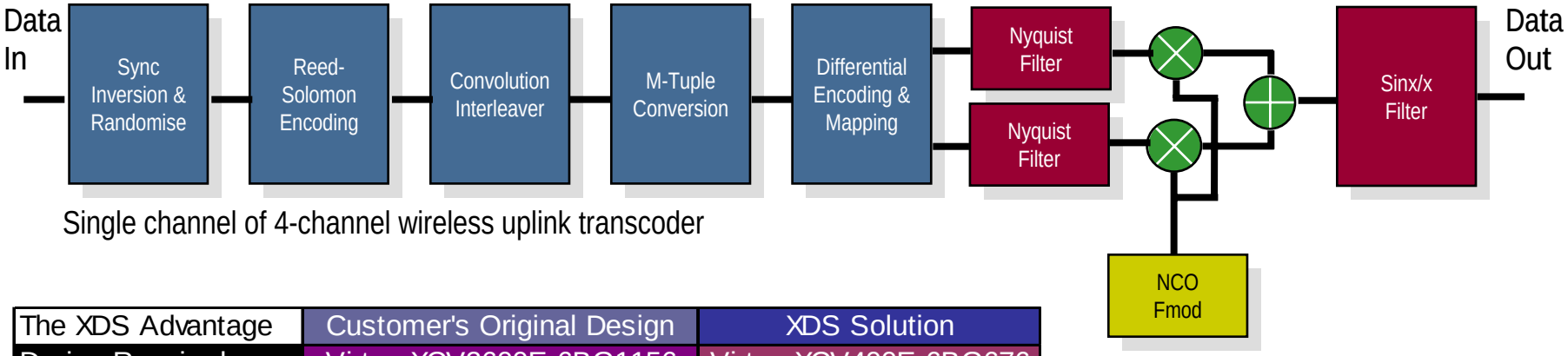
Multiple Channels on the Platform FPGA



- Think 3D rather than 2D when designing
  - Reuse resources by multiplexing if extra horsepower available
    - e.g. If running half the max speed of FPGA, you could do twice as much in same period
  - Support multiple channels in less FPGA resources than you'd expect

XDS Case Study

DESIGN SERVICES
Xilinx Global Services



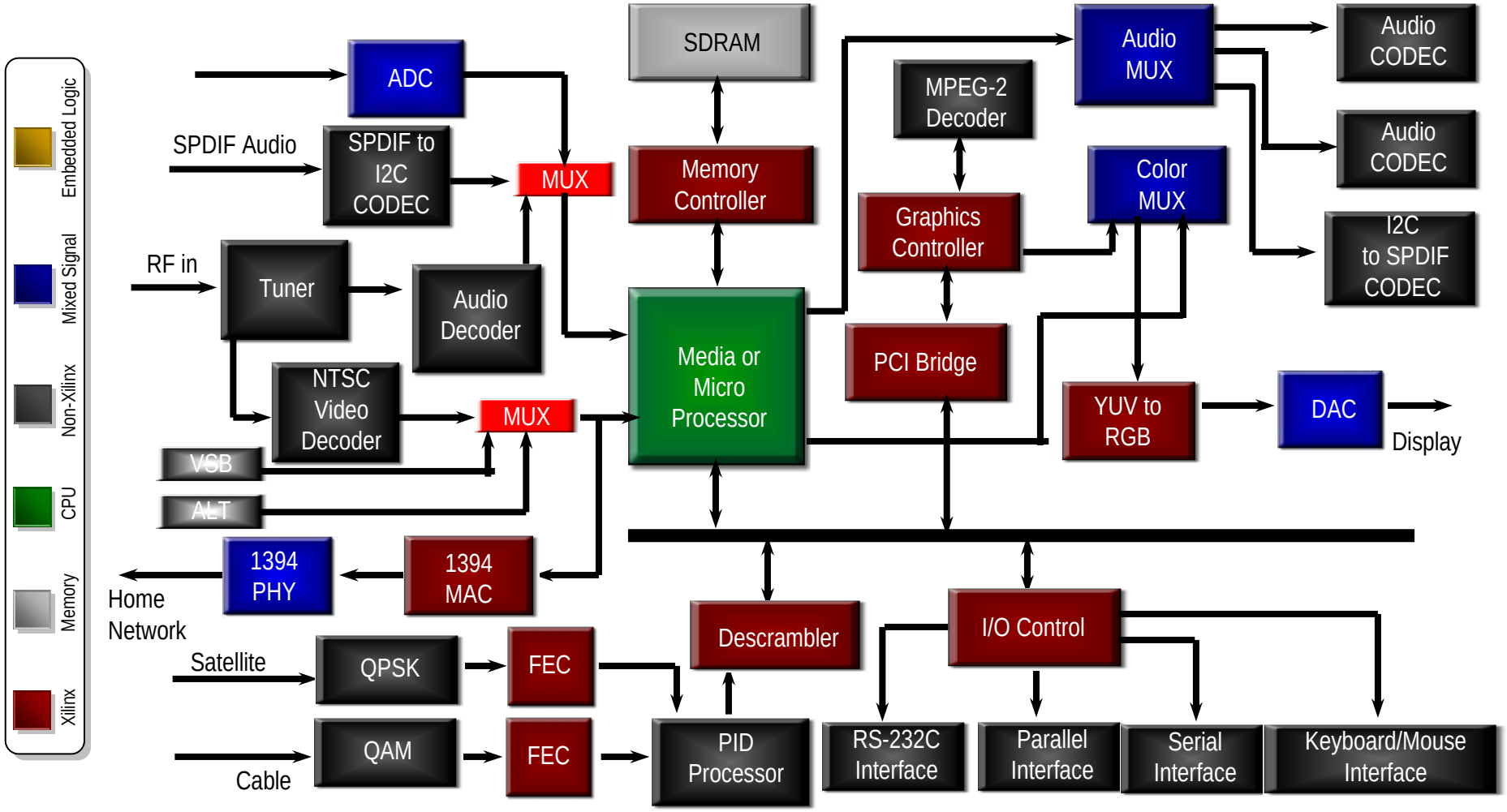
Single channel of 4-channel wireless uplink transcoder

The XDS Advantage	Customer's Original Design	XDS Solution
Device Required	Virtex XCV2600E-6BG1156	Virtex XCV400E-6BG676
Cost*	$12X	$X

- Xilinx Design Services (XDS) solution delivered >90% savings on device price over original design!
  - Relatively slow speed of four paths through FPGA allowed multiplexing
- Use of Xilinx FPGA enabled customer to prototype their product within 4 months
- Customer able to recover one-time development cost before prototype completion
- Engaging XDS enabled customer to develop successful product with viable cost structure and faster time-to-market

*(100+ pricing for comparative purposes only)

Example DVB Receiver System



For more detailed presentations on set top boxes & receivers, check out www.xilinx.com

Conditional Access

- Three key parts to Conditional Access (CA)
  - Scrambling/Descrambling
    - Making the service incomprehensible to unauthorised users
  - Entitlement Checking
    - Providing the access requirement information to users
    - Providing a decryption key to authorised users
  - Entitlement Management
    - Distributing entitlements to receivers

- Xilinx is extremely successful in cryptography (DES, TDES & AES)
  - Relatively low device utilisation and high (Gigabit/s) throughput
  - Faster than any software!
  - Programmable : able to update regularly and on-the-fly
  - Extra level of security can be added as a wrapper

Xilinx Cryptography Solutions

- Spartan-3 encryption solutions are NIST approved
- The programmable nature of these solutions allows easy customization based on end application requirement

	Spartan-IIE Solution			
	DES	Triple-DES	AES	AES
Device	2S100E-6	2S150E-6	2S100E-6	2S100E-6
CLB Slices	235	1611	358*	231**
Performance	94 MHz	48 MHz	82 MHz	82 MHz
Area Utilization	19.58%	93.22%	29.83%	19.25%
Key Size	56-bit	128-bit or two 64-bit	128/192/ 256-bit	128/192/ 256-bit

AES aims to replace DES over long term
Program now with DES and replace with AES later via network

Note: Solution includes encryption, decryption and key generation * 128-bit key implementation ** Key Generation offloaded to embeddedμC/ μP

DVB-RCS Turbo Decoder Core

- Interactive Return Channel for Satellite customers
- Xilinx Alliance core partner iCODING offers high performance, flexible solution based on turbo coding error correction
  - Fast time-to-market
  - Updateable if the new standards change during development

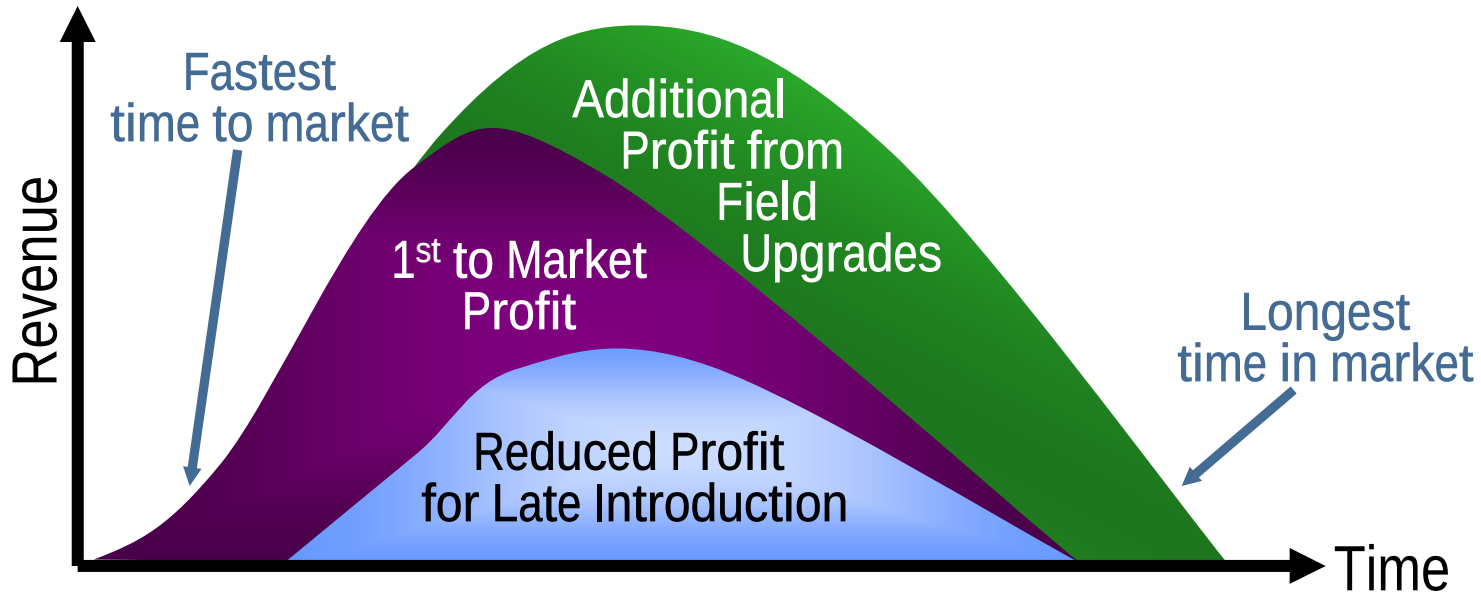
iCODING™ technology incorporated

Alliance CORE™

Supported Family	Device Tested	CLB Slices	Clock IOBs[1]	IOBs[1]	Performance (MHz)	Xilinx Tools	Special Features
Virtex-II	2V2000-5	5801	1	35	69	3.3i	15 BlockRAMs
Virtex-E	V2000E-8	5265	1	35	43	3.3i	29 BlockRAM

Notes:
1. Assuming all core I/Os are routed off-chip

Time-to-Market Value



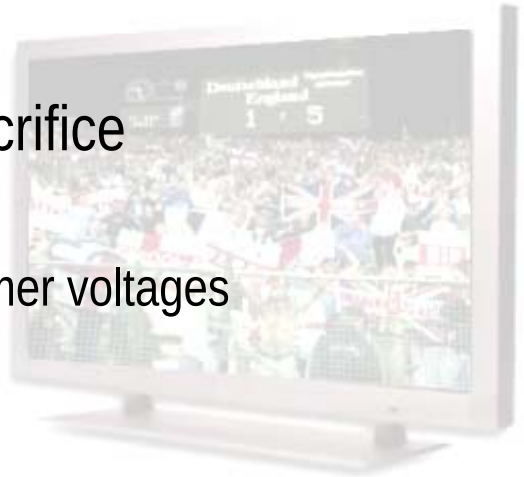
Quicker time to market and reprogrammability provide the best chance of achieving full product profit potential

Transmitter Solutions

- Xilinx offers IP solutions for
  - Forward Error Correction (FEC)
  - Content encryption and energy dispersal scrambling
  - COFDM modulator and baseband shaping
- Integration of multiple channels on single device
  - Lower BOM
  - Lower cost-per-channel
- Higher performance with XtremeDSP
  - Increased bandwidth and more from available bandwidth
  - Reduce size of “DSP farms”
- Total flexibility
  - Fast time-to-market and differentiation
  - Tuneable solution to different broadcast requirements

Receiver Solutions

- Xilinx CPLDs and FPGAs provide time-to-market and flexibility advantages for receiver systems
  - Quickly interface receiver chipsets to host processor without waiting for ASSP/ASIC re-spin
  - Or add extra features to receiver units, like hard drive or smart card reader
- Ease of integration
  - Small packaging and minimal thermal impact
- Power saving benefits without performance sacrifice
  - Operating mode and battery management
  - Support higher automotive voltages or lower consumer voltages
- Adds additional performance
  - Reduce processor workload by handling interfaces
  - Expand microprocessor I/O

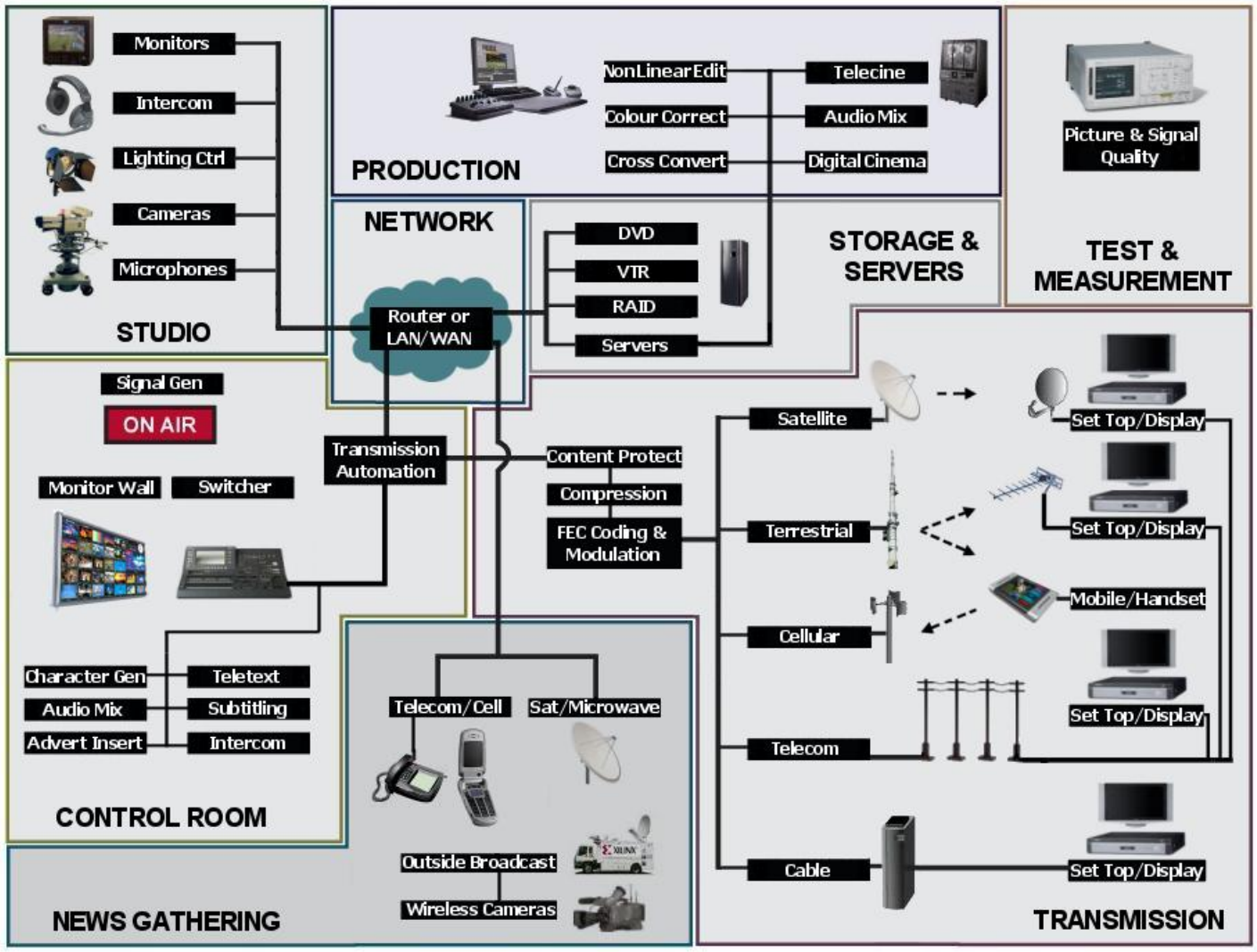


Xilinx Transmission Solutions

- Xilinx offers programmable solutions at all digital stages of the DVB, ATSC, ISDB, DMB & DAB transmit and receive chains
- Multi-channel support available on one chip
  - Parameterisable FEC cores available now
- Plenty of gates available for “back-end” designs and value add functions for complete system-on-chip solution
  - Other DSP blocks including filters and image processing cores
  - Network interface cores available
- Reprogrammability also gives flexibility
  - Faster time-to-market
  - Longer time-in-market
- Xilinx Design Services can help for bespoke solutions

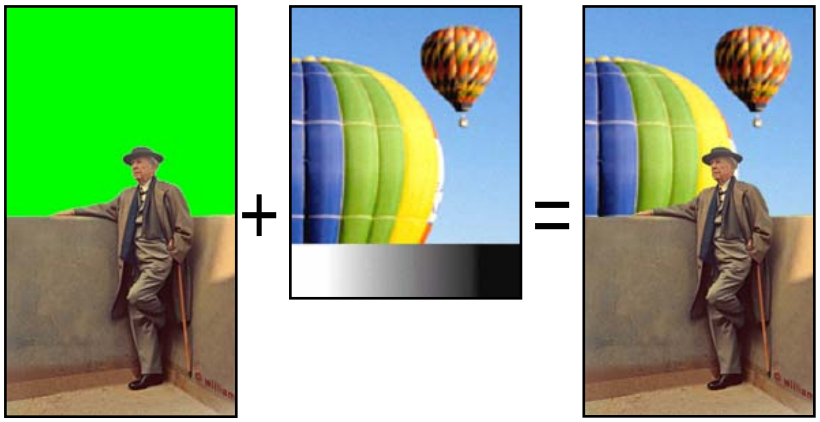
Xilinx in the Broadcast Chain

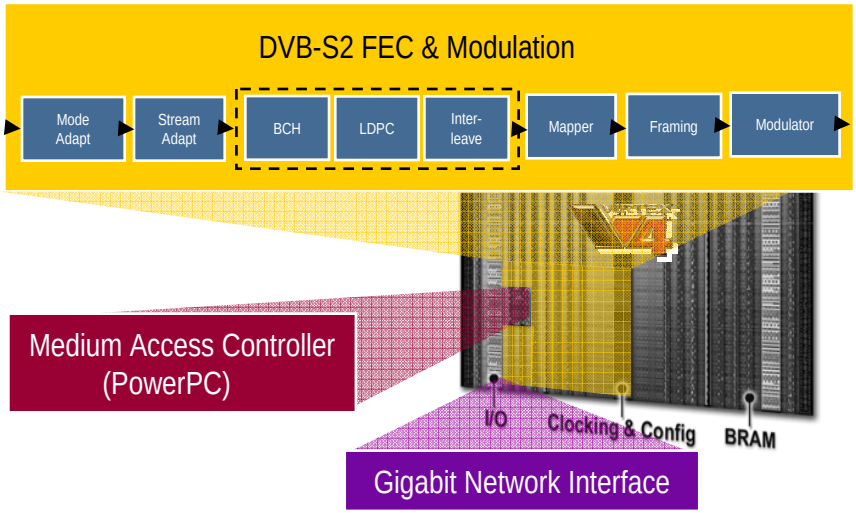
- Gamma Correction
- Codecs
- Scaling/Resampling
- Colour Space
- Network Interfacing
- Chip Interfacing
- Video Filtering
- Effects (Wipe/Key)
- Memory Control
- FEC/Modulation
- System Control



Real Time HD/Multichannel DSP

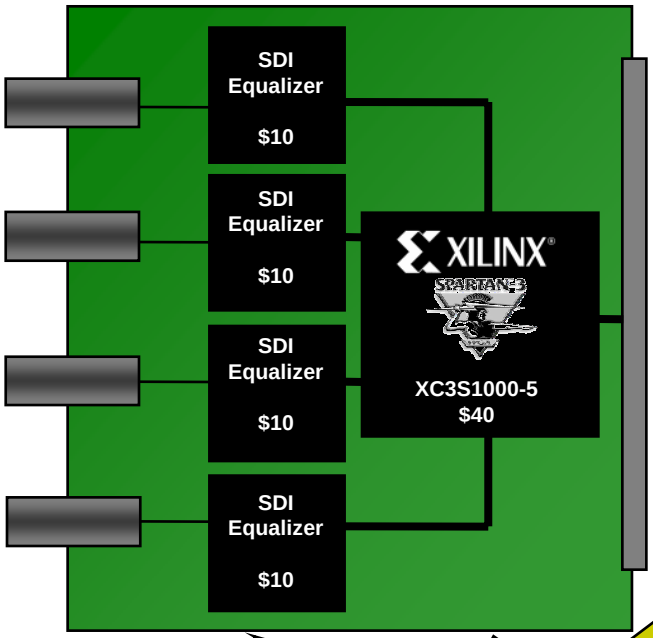
- Highest performance on-chip DSP blocks, multipliers and memory
- Reduce size of DSP farms
- Support real time HD processing
- Support multiple channels of SD processing through resource sharing
- Reduce cost-per-channel for FEC and modulation





Cost Effective Connectivity

- Significant cost-per-channel reductions
- Portfolio of audio/video connectivity solutions
  - SDI, HD-SDI and DVB-ASI
  - Video-over-IP
- Wide range of general telecom, datacom and backplane solutions available
  - Ethernet, PCI Express, ATM, Fibre Channel, SONET, SPI RapidIO, HyperTransport…



~70% cheaper than ASSP SDI solutions!

Flexible Embedded Processing

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- Simple state-machines and “localised” on-chip control
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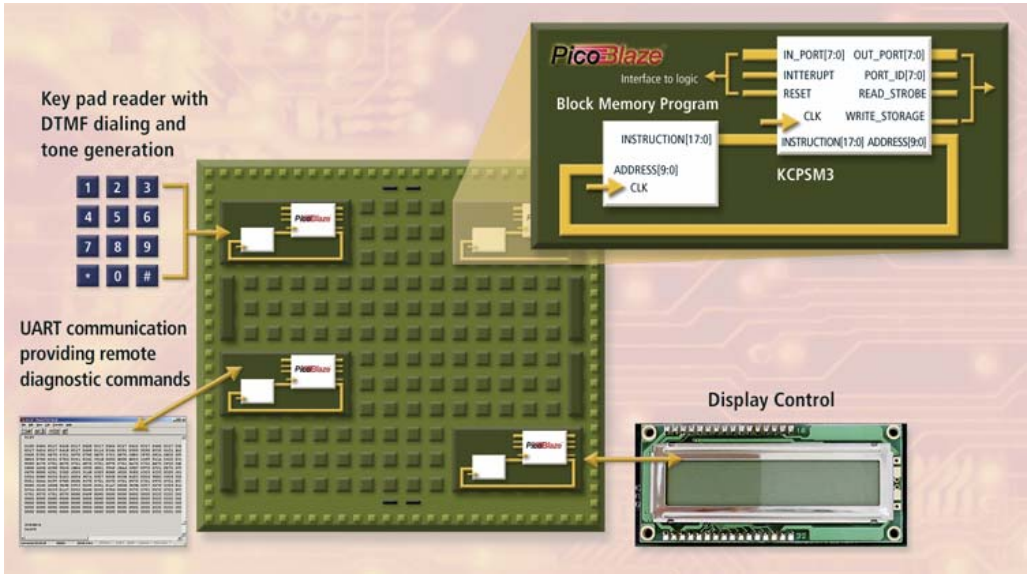

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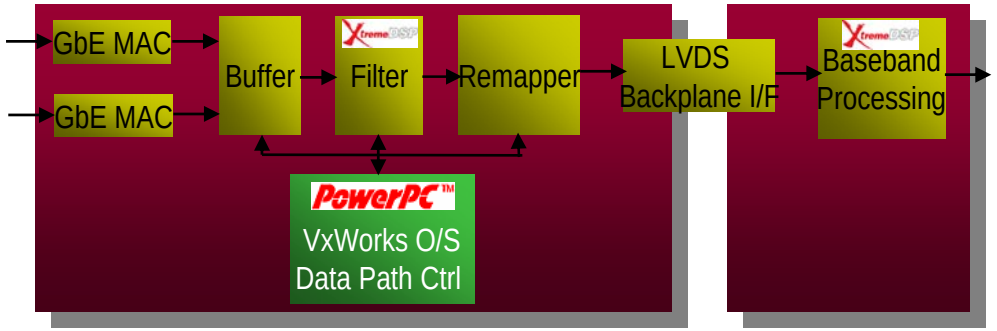
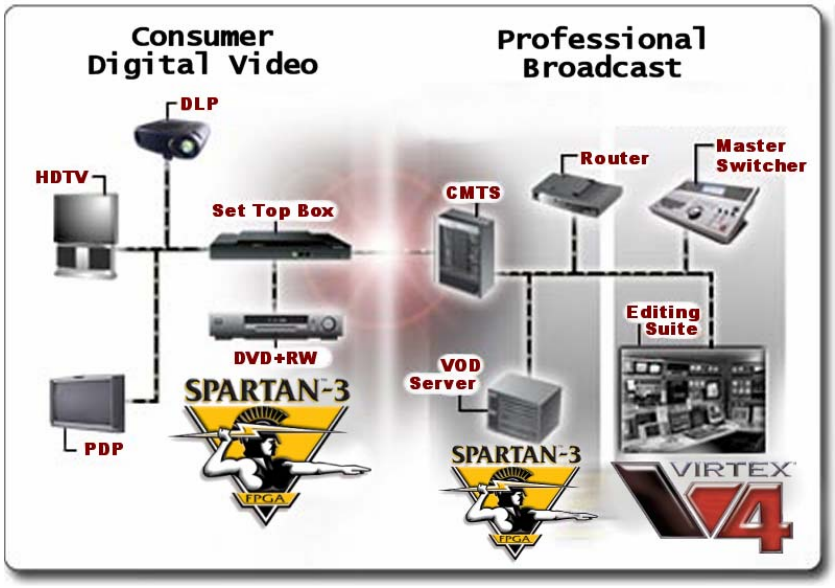
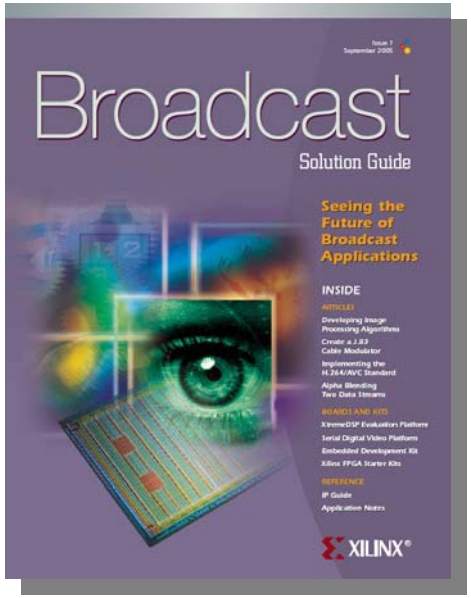


Xilinx in Broadcast

Programmable Solutions for the Broadcast Industry





Interfaces & Connectivity Codecs Video & Audio Processing Transmission & Reception End Applications

More info on a wide range of applications and technologies

www.xilinx.com/broadcast