Operation of a 1-bit Quantum Flux Parametron shift register (latch) by 4-phase 36-GHz clock

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Abstract—**The Quantum Flux Parametron (QFP) is a SFQ-type logic device which uses a single flux quantum (SFQ) to represent 1-bit of information. QFP circuits use a multi-phase external ac power which also acts as the clock for synchronization, hence QFP circuits are highly pipelined. The clock frequency must be increased to improve the throughputs of the circuits, so the control of a high frequency clock is a key technology for the QFP. This paper describes a clock distribution technique which utilizes the characteristics of a standing wave. Using this technique, the operation of a 1-bit QFP shift register by a 4-phase clock up to 36 GHz is shown. In the 4-phase clock operation of QFPs, the input is given in phase 1, the QFP switches in phase 2, the output is held during phase 3, and the QFP resets in phase 4. Therefore, the 4-phase 36-GHz operation means that each QFP switches or resets in less than 7 ps.**

I. Introduction

Single Flux Quantum (SFQ) type devices are receiving much attention because of their extremely high throughputs and very low power consumption [1-3]. One of the major problems in SFQ devices is the method of synchronization caused by their high throughputs. In the case of the Quantum Flux Parametron (QFP), one type of SFQ logic device, a multi-phase external ac power is used which also acts as the clock for synchronization [4-9]. The clock frequency must be increased to improve the throughputs of the circuits, so the control of a high frequency clock is a key technology for the QFP. It is technically difficult to distribute a high frequency (>1 GHz) clock, so asynchronous systems are proposed for RSFQ logic (another type of a SFQ logic) [1]. Such asynchronous systems can work at more than 100 GHz locally, but if interactions with other systems (e.g. I/O operations) are required, synchronized systems are more effective. So high frequency clock distribution at more than 10 GHz must be achieved to enjoy the merits of a SFQ logic system.

In order to show a high frequency clock distribution that is capable of exploiting potentials of the QFP, we have reported the operation of a 1-bit QFP shift register up to 16 GHz [10]. Crosstalk with the clock signal is the major disturbance in the measurement. The aims of this paper are:

(1) to show that this crosstalk can be reduced by actively using the characteristics of a standing wave which is a unique clock distribution scheme for QFP circuits, and
(2) to demonstrate faster operation of the QFP shift register by using this scheme.

The paper first presents a brief review of the QFP shift register. This is followed by the powering (clock distribution) system of QFP logic circuits. Finally, the high frequency operation of the QFP shift register is described.

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II. QFP shift register

Shift registers are very useful and indispensable devices in many signal processing applications [11]. Previously, the QFP shift register has been reported [10], but for the reader's convenience, the design and the operation are briefly reviewed in this section. The detailed operation of the QFP can be found in [3].

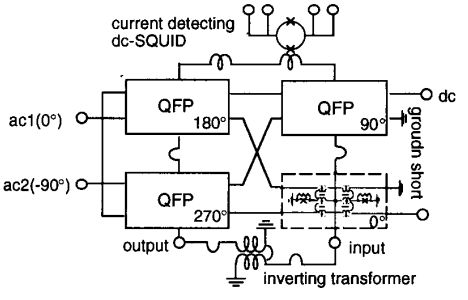

Fig.1 One-bit cell of QFP shift register. A 1-bit shift register is made by cascading four QFPs. In order to simplify the QFP testing, the circuit includes a bit inverting transformer to produce subharmonics of the clock frequency. The current circulating along the QFP loop is measured by using a damped dc-SQUID which is biased in the voltage region.

Fig. 1 shows the structure of a single-bit shift register cell. This cell is made by cascading four QFPs which are driven by four-phase sine-wave clock signals. Two phases (ac1 and ac2) are provided externally, and the four-phase clock is produced on-chip by applying a dc flux bias to the QFPs. The operation of a single-bit shift register cell can be understood as follows. At the beginning of the clock cycle the first QFP (0°) is activated shifting the logic bit from the input of the shift register to the input of the second QFP (90°). After that the second QFP is turned on shifting the logic state to the input of the third QFP (180°) and in the meantime the first QFP is deactivated. The same step is next applied to the third QFP. At the end of the clock cycle the fourth QFP (270°) is activated shifting the logic bit to the output of the shift register. The output of the shift register is fed back into the input through the inverting transformer to produce subharmonics of the clock frequency. So this circuit operates just like a frequency prescaler. This scheme enables simple measurement because the output can be easily recognized in spite of the existence of crosstalk with the clock signal and broadband white noise of the microwave output amplifier. The current circulating along the QFP loop is measured by using a damped dc SQUID. The dc SQUID biased in the voltage state is used because it causes negligible disturbance to the QFPs.

III. Powering System

Performance of many LSI circuits is hampered by the clock distribution network and not by the individual devices' intrinsic limiting frequencies. The major problems are clock skew, power dissipation in the clock distribution network and crosstalk with the clock signal. This section first introduces a unique standing wave method for QFP circuits, which realizes a skew-less and low-power clock distribution. Next described is a new crosstalk cancellation technique achieved by actively using the node of a standing wave. The crosstalk can be alleviated by using a multi-phase clock [12], but the effects are limited because the impedance mismatch around a chip boundary which is the major cause of a crosstalk is hard to be controlled. The standing wave technique makes a stable and accurate measurement possible and very high frequency operations are achieved as shown in the next section.

The QFPs are clocked using a standing wave to realize a low power clock distribution and to guarantee global synchronization. Conventionally, the clock power is distributed using a resistive network. Such clock schemes are the main contributors to power dissipation in the case of Josephson voltage state logic. In the standing wave distribution scheme, no resistors are used in the clock line, so

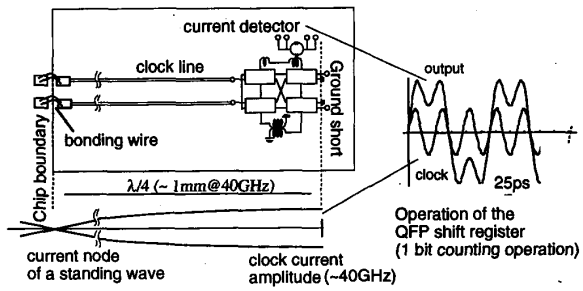

Fig.2 Clock distribution by using a standing wave. A standing wave is used to avoid a clock skew and to guarantee the global synchronization. Moreover, a crosstalk between the output and the clock can be alleviated by utilizing the current node of the standing wave.

only the QFPs (and detecting SQUIDs) are the on-chip contributors to power dissipation. Global synchronization is realized because the phase of a standing wave is the same along the whole wave. Hence the clock skew problem does not exist intrinsically. The standing wave is obtained by shorting the end of the clock lines (Fig. 1, 2). Because a standing wave is used, the clock current amplitude is not constant along the clock lines. It is at its maximum at the short and decreases with increasing distance from the short until it vanishes when the length is $\lambda/4$, where λ is the wave length of the clock signal. This means that the clock current amplitude received by each QFP varies according to its position along the clock line. It is found that the QFP can be clocked at multi-gigahertz frequencies within an electrical current amplitude margin of about 20% [10]. If the QFPs are to be powered within a 20% margin, the clock line length along the QFP circuit should not exceed $\lambda/16$. In order to alleviate this restriction, the QFPs can be powered in parallel by using an inductive tree [7]. Also it should be noted that the size of the synchronous area is the order of the wave length of the clock signal, because the signal must be propagated from corner to corner of the synchronized region within one clock cycle.

The chip containing the QFP circuits is wire-bonded to a ceramic carrier. The return current through non-negligible self-inductance of the wire bonds produces voltage oscillations of the clock ground plane. This is the origin of crosstalk with the clock signal which can be 1000 times as large as the output of the detecting SQUID. For reducing the crosstalk, the ground planes of the clock network was separated from other grounds [10]. Nevertheless, they were still capacitively coupled and the crosstalk was not completely removed. So we decided to use the current node of a standing wave actively to eliminate the crosstalk. If the position of the wire bond is adjusted to be located at a distance of $\lambda/4$ from the short, the current amplitude across it can be minimized. This implies a minimum in the amplitude

of voltage oscillations of the clock's ground plane. This technique is very powerful as shown in the next section. The accurate powering condition and the stable circuit operation are realized by this method.

IV. High Frequency Operation

The experimental set-up is almost the same as that used in [7] except that microwave components corresponding to higher frequency are used. The two phases of the clock lines are adjusted by using phase shifters (adjustable delay lines). The clock amplitude is modified by the microwave signal generator output power and the dc-offset current. The amplitude unbalance of two clock signals can be controlled by using attenuators, but the adjustment is usually unnecessary if the two clock lines are designed symmetrically.

Fig. 3 shows the output spectrum of the shift register shown in Fig. 1. The Josephson junction is fabricated using a standard Nb trilayer process with a lateral size definition of 2 μm and a critical current density of 2800A/cm^2. The measurements are done by using a spectrum analyzer with a resolution- and a video-bandwidth of 10 KHz. The noise floor is limited by the microwave amplifiers. The device is able to operate at a clock frequency as high as 36 GHz. Because this circuit produces subharmonics of the clock signal, the output of 18 GHz is observed. To the best of our knowledge it is the fastest external clock frequency for superconducting circuits. The frequency is limited by the bandwidth of the microwave amplifier used in the experiment and not by the intrinsic operating speed of the circuit. According to computer simulations, the 1-bit shift register cell should work at more than 70 GHz.

Very sharp and stable subharmonics can be obtained only when suitable powering conditions predicted from the low

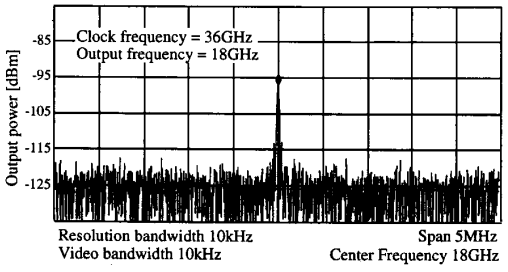

Fig.3 Output spectrum of the 1-bit QFP shift register at clock frequency of 36GHz. Because the circuit includes a bit inverting transformer, the output of 18GHz spectrum is obtained. The shown power is subtracted by the amplifier's gain. The resolution bandwidth is 10 KHz and a video bandwidth is 10 KHz. The noise floor is limited by the microwave amplifiers

TABLE I
Operating Margin of QFP Shift Register

	ac1	ac2	dc
Low frequency operation (~10KHz)	0.58[mA] ±0.48(83%)	0.59[mA] ±0.48(81%)	0.78[mA] ±0.48(61%)
	ac (= ac1+ac2)		dc
High frequency operation (~20GHz)	-15.2[dBm] ±2.8(dBm)	1.43[mA] ±1.08(76%)	0.67[mA] ±0.10(15%)

frequency experiments are satisfied (Table I). This implies that the obtained subharmonics is the output spectrum of stable and correct operation (and is not a resonance). In the 4-phase clock operation of QFPs, the input is given in phase 1, a QFP switches in phase 2, the output is held during phase 3, and the QFP resets in phase 4. Therefore, the 4-phase 36-GHz operation means that each QFP switches or resets in less than 7 ps.

Table I shows the typical operating (bias) margins of the shift register at high frequency (~20GHz) and low frequency (~10kHz). The margin at low frequency agrees well with the result of the static analysis. The margin at high frequency sometimes decreases as shown in the table. The reason is considered to be ground bounce caused by the inductance of the bonding wire which makes the control of the microwave power very complicated.

A tremendous reduction of the crosstalk between the clocks and the detector's output is observed when clocking the QFP at the frequency corresponding to a wire-bond to short distance of $\lambda/4$. Fig. 4 shows the measured and calculated crosstalk power of the shift register circuit.

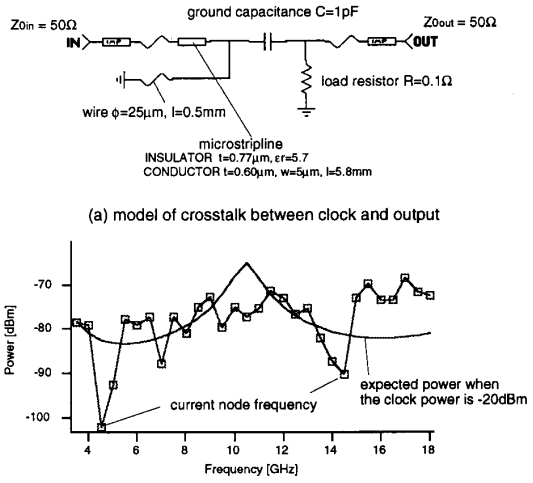

Fig.4 The model of QFP powering system and the numerically/experimentally obtained crosstalk power. The crosstalk power is minimized when the electrical length of the clock line becomes 1/4 of the wave length of the clock.

The calculation used a simple transmission line model with the inductance of the bonding wires and the lumped resistor representing all devices in the circuit. Both results show that the crosstalk power spectrum has a local minimum when the clock frequency satisfies the above condition of the crosstalk reduction. This scheme is actively used for the measurements of 36GHz operation because the ground bounce is minimized and the powering condition can be easily found.

V. Conclusion

In order to demonstrate a clock distribution scheme that is capable of exploiting the potentials of the QFP, a standing wave distribution scheme was used for powering the QFP shift register. Low-power and skew-less distribution can be realized by this method. Moreover, by actively using the current node of a standing wave, a tremendous reduction of the crosstalk between the clocks and the detector's output is shown to be possible because the ground bounce caused by the return current through the bonding wires can be minimized.

The standing wave clock distribution enables the 1-bit shift register cell to operate at a clock frequency as high as 36 GHz. Accurate powering condition and stable circuit operation are realized by active cancellation of the crosstalk.

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