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Design and implementation of a high-speed bit-serial SFQ adder based on the binary decision diagram

Kenji Kawasaki[1], Kenichi Yoda[1], Nobuyuki Yoshikawa[1], Akira Fujimaki[2], Hirotaka Terai[3] and Shinichi Yorozu[4]

[1] Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya-ku, Yokohama 240-8501, Japan
[2] Department of Quantum Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
[3] Communication Research Laboratory, 588-2 Iwaoka, Nishi-ku, Kobe 651-2492, Japan
[4] SRL-ISTEC, 34 Miyukigaoka, Tsukuba 305-8501, Japan

E-mail: yoshi@yoshilab.dnj.ynu.ac.jp

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Abstract
We have designed a high-speed SFQ bit-serial carry-save adder based on the binary decision diagram (BDD). A simple bit-serial carry-save adder based on the BDD we first designed has a carry-feedback loop. Its input data frequency is limited by the propagation delay in the feedback loop. In our second adder design, we have replaced one BDD gate with a nondestructive binary switch, by which we can eliminate the carry-feedback loop. We have designed the high-speed BDD SFQ bit-serial adder using the NEC 2.5 kA cm^{-2} Nb standard process and the CONNECT cell library. The circuit simulation indicates that the maximum operating frequency is 38 GHz and the dc bias margin at 10 GHz is ±23%. We have confirmed its correct operation in the on-chip high-speed test. The maximum operating frequency was found to be 23.8 GHz.

1. Introduction

Rapid single flux quantum (RSFQ) logic circuits [1] are promising circuit technology because of their high-speed and low-power operation. We have been developing a bit-serial SFQ microprocessor, where its speed is mostly limited by a bit-serial full adder. Many serial adders have been studied and are reported in [1–4]. In this study, we have investigated a bit-serial SFQ adder architecture based on the binary decision diagram (BDD) [5] to increase an input data frequency. The BDD SFQ circuits are a data-driven self-timed (DDST) system [6], and have the following advantages: (i) the timing design is simple due to its asynchronous nature and (ii) the propagation delay is small because of their small gate counts. Our first adder design uses a one-bit BDD adder with a carry-feedback loop, whose input data frequency is limited by the propagation delay in the carry-feedback loop. In our new adder design, we eliminate the carry-feedback loop in order to increase the input data frequency. We have implemented the high-speed bit-serial adder and tested it at high speed.

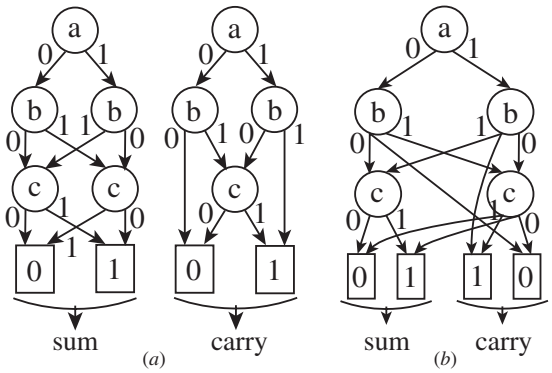

Figure 1. A binary decision diagram (BDD) of a one-bit full adder. (*a*) A sum and a carry are calculated separately. (*b*) Common nodes are combined together.

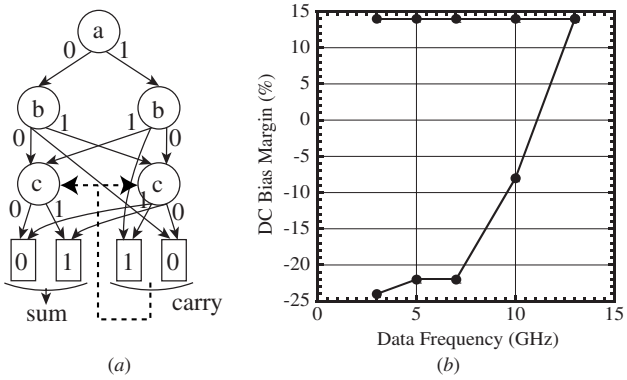

Figure 2. A bit-serial carry-save BDD adder with a carry-feedback loop. (*a*) A BDD representation. (*b*) The dependences of the upper and lower bias margins of the adder on the input data frequency.

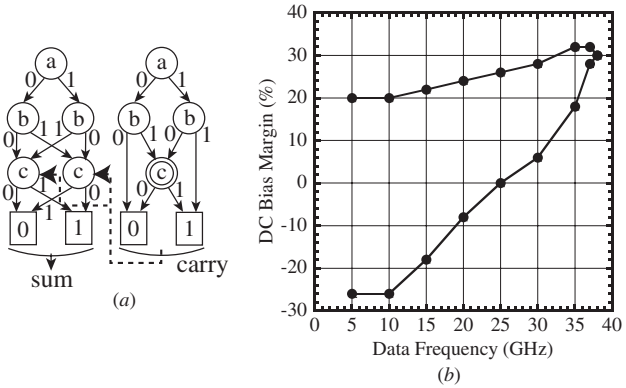

Figure 3. A high-speed carry-save BDD adder without a carry-feedback loop. (*a*) A BDD representation. A double circle denotes the nondestructive version of the Bina cell. (*b*) The dependences of the upper and lower bias margins of the adder on the input data frequency.

2. Adder design based on the binary decision diagram

Figure 1(*a*) shows the BDD representation of a sum and a carry of a one-bit full adder [5]. The BDD is a directional graph, which is composed of many binary switches (nodes) with one input and two outputs. Each node switches the input SFQ pulse into one of two directions depending on its internal state as designated in the figure. The internal state of the node is defined by the dual-rail input (it is not shown in the figure) before the input of the SFQ pulse. The result of the calculation of the BDD adder corresponds to the final destination of the

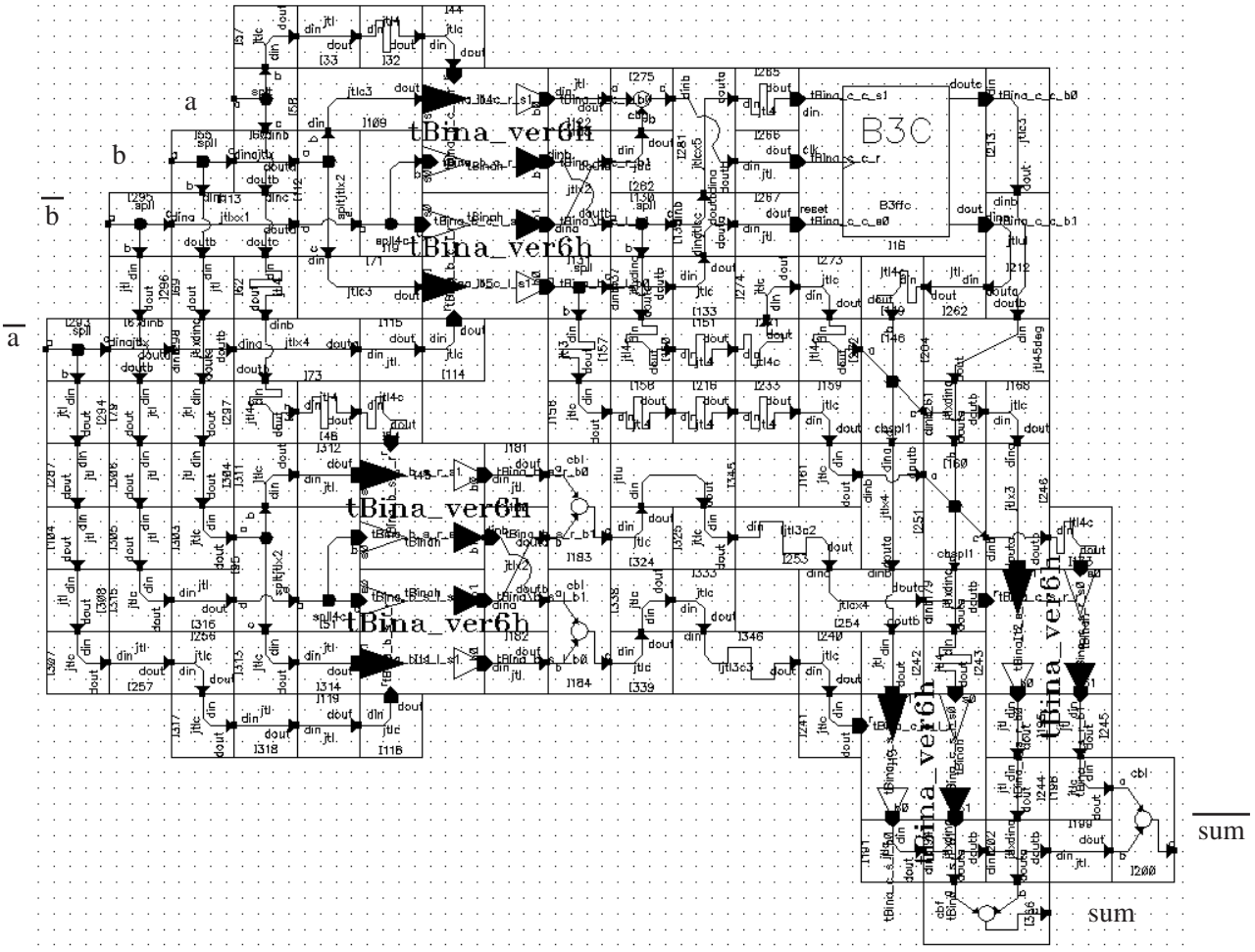

Figure 4. A circuit schematic of the high-speed carry-save BDD adder without a carry-feedback loop.

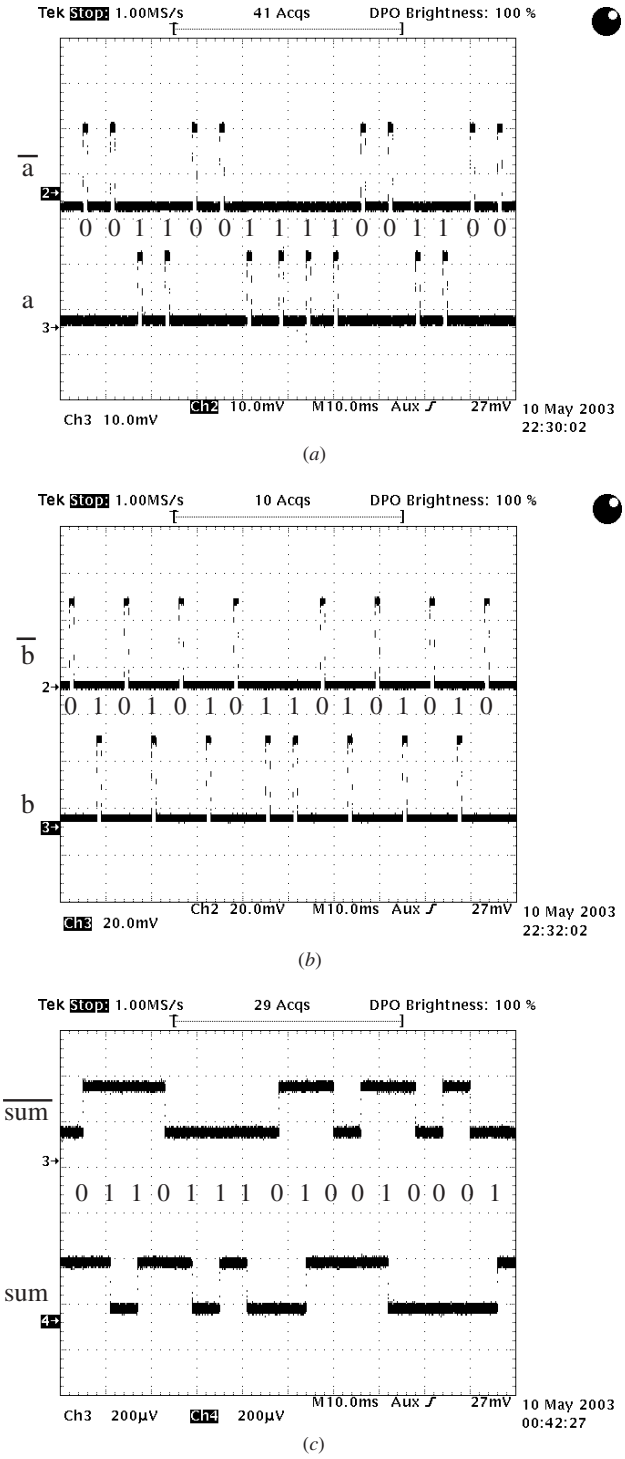

Figure 5. Low-speed test results of the high-speed carry-save BDD adder. Each rising edge corresponds to an input of an SFQ pulse for 'a', '$\bar{a}$', 'b' and '$\bar{b}$'. Each transition corresponds to an output of an SFQ pulse for 'sum' and '$\overline{\text{sum}}$'. (a) and (b) display the input data sequence
$a = (0011001111001100)$ and $b = (0101010110101010)$, respectively. (c) is the output data of sum $= (0110111010010001)$.

SFQ pulse, which is denoted by '0' or '1' in the box. The one-bit BDD full adder can be simplified furthermore by combining the nodes with the common function as shown in figure 1(b).

2.1. Carry-save adder with a carry-feedback loop

A simple way to make the one-bit BDD full adder in figure 1 into a bit-serial carry-save adder is by just adding a carry-feedback loop as shown in figure 2(a). The carry-feedback loop is designated in the figure as a dotted line. We have designed this type of adder using CONNECT cell library [7], and evaluated its performance by circuit simulations. The Bina cell [5], which is a destructive delay flip-flop with a dual-rail input and output, was used as the binary switch in the BDD. Figure 2(b) shows dependences of the upper and lower dc bias margins on the input data frequency obtained from circuit simulations, where NEC Nb 2.5 kA cm^{-2} process is assumed. The simulation results show that the maximum input data frequency is 13 GHz, which is limited by the propagation delay in the carry-feedback loop.

2.2. High-speed carry-save adder without a carry-feedback loop

A close observation of the carry-feedback loop in figure 2(a) brings about the idea that the feedback loop can be eliminated in the adder by replacing the lower right node with a nondestructive delay flip-flop because its next internal state is just the same with the current state. Such a new carry-save adder is presented in figure 3(a), where the nondestructive version of the Bina cell is denoted by a double circle in the figure. Figure 3(b) shows the dependence of the dc bias margins of the high-speed carry-save adder without the carry-feedback loop on the input data frequency, which is obtained by the circuit simulations. The circuit is designed by using the CONNECT cell library and the NEC Nb 2.5 kA cm^{-2} process. As can be seen in the figure, the maximum input data frequency is increased up to 38 GHz by eliminating the carry-feedback loop.

3. Test results

We have implemented the high-speed bit-serial adder without the feedback loop using the NEC Nb 2.5 kA cm^{-2} process and tested it at low speed. A circuit schematic of the BDD adder is shown in figure 4. The adder contains 513 Josephson junctions and its size is 600 μm $\times$ 720 μm. Figure 5 shows its test results at low speed, where dual-rail bit-serial data, $a = (0011001111001100)$ and $b = (0101010110101010)$, are inputted. We can clearly see that sum $= (0110111010010001)$ are obtained correctly. The low-speed dc bias margin is found to be -16.5%–$+19.1\%$.

We have also tested the adder at high speed using the on-chip high-speed test system [8]. Figure 6 shows a circuit schematic of the system. The system is composed of two four-bit DDST shift registers for loading the data, one four-bit DDST shift register for reading the data, and a four-bit clock generator (CG) to provide a high-speed clock to the input shift registers. The on-chip high-speed test is performed as follows: first, input data are loaded to the input shift registers at low speed (denoted as (1) in figure 6). Then a CG trigger pulse is applied to the CG, which generates a four-bit high-speed clock and provides it to the input shift registers ((2) in the figure). This high-speed clock pushes the data in the shift registers, which send the data pulses to the adder at high speed

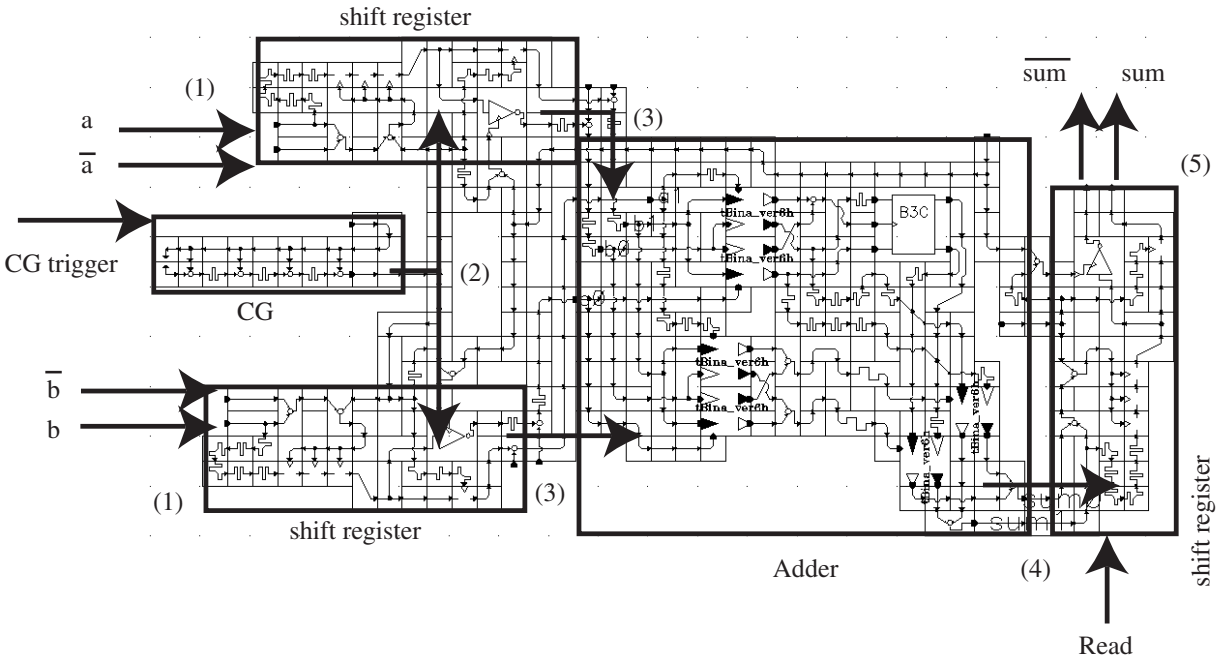

Figure 6. A circuit schematic of the on-chip high-speed test system.

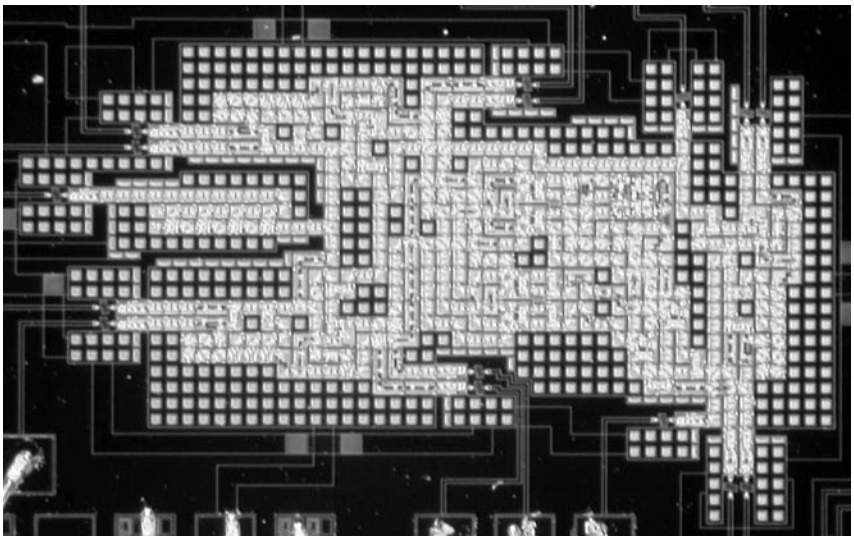

Figure 7. A photograph of the on-chip high-speed test system.

((3) in the figure). Output data calculated by the adder are sent to the output shift register at high speed simultaneously ((4) in the figure). Finally the data in the output shift register are read out by applying the read pulses to the output shift register at low speed ((5) in the figure). A photograph of the on-chip high-speed test system is shown in figure 7. The system contains 1434 Josephson junctions and its size is 1200 μm $\times$ 2040 μm.

Results of the on-chip high-speed test at 16 GHz are shown in figure 8, where dual-rail bit-serial data, $a = (1100)$, $b = (1010)$ and $a = (1001)$, $b = (1010)$, are inputted successively. One can clearly see that output data, sum $=$ (0001) and sum $=$ (0111), are obtained correctly. We have estimated the frequency of the CG by the circuit simulation. Separate high-speed measurement of the CG shows that the tested frequency agrees well with the circuit simulation results [9]. The operating margins of the adder were also examined at various frequencies by changing the bias current of the CG independently. Figure 9 shows the dependences of the upper and lower margins of the adder on the data input frequency. Simulation results are also plotted in the figure for comparison. The maximum frequency of the adder was found to be 23.8 GHz from the on-chip high-speed test.

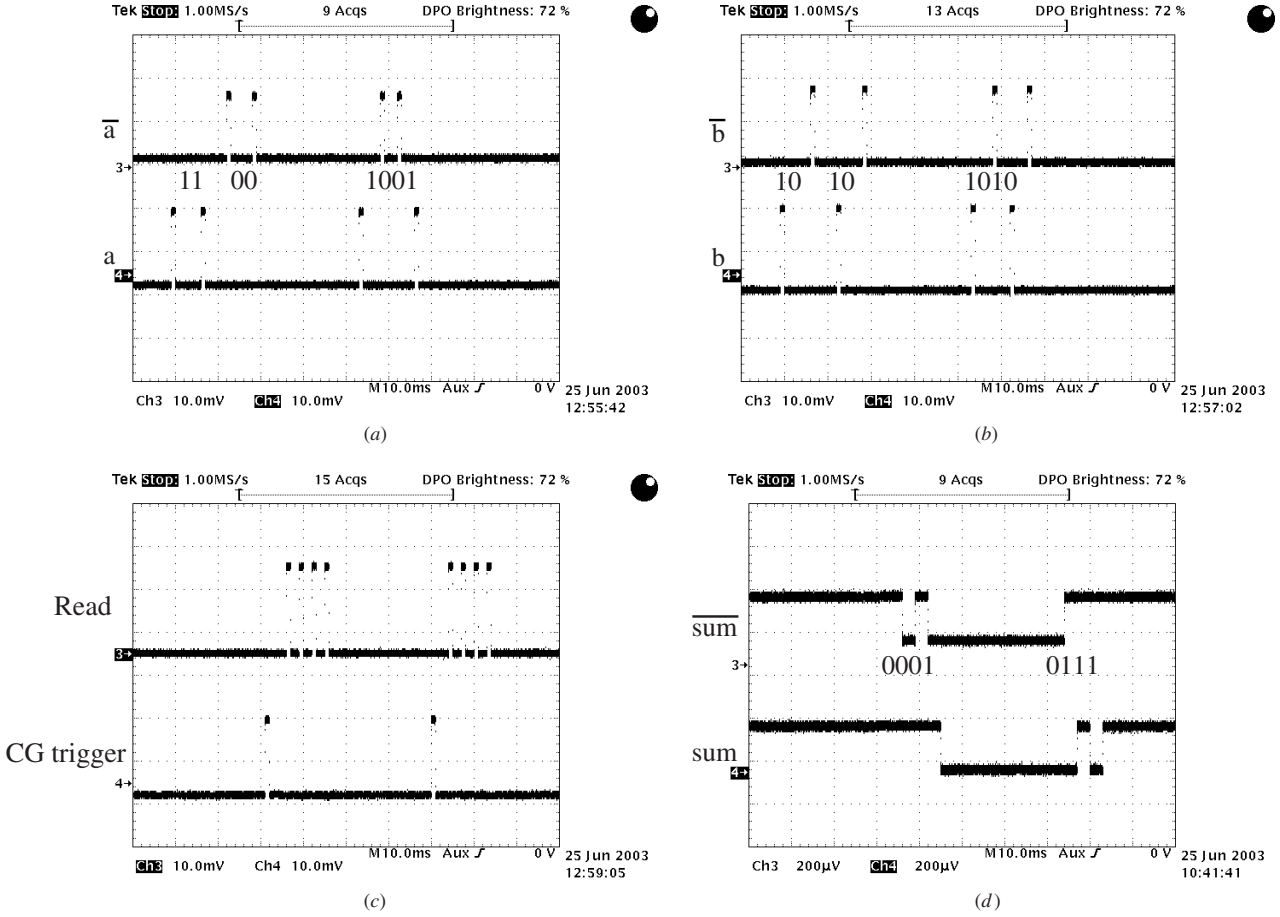

Figure 8. High-speed test results of the high-speed carry-save BDD adder. Parts (*a*) and (*b*) display the input data $a = (1100)$, (1001) and $b = (1010)$, (1010), respectively. Part (*c*) is the read and CG trigger pulses. Part (*d*) is the output data, sum = (0001), (0111).

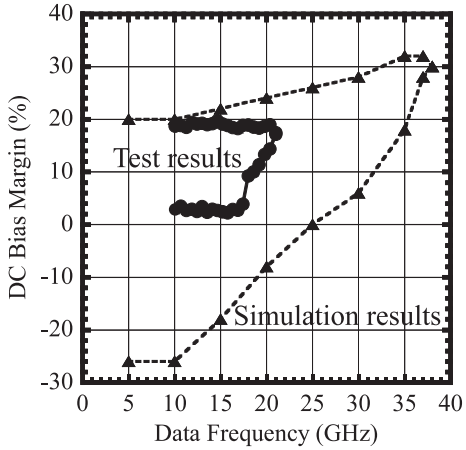

Figure 9. The dependences of the upper and lower bias margins of the high-speed carry-save BDD adder on the input data frequency obtained by the high-speed tests and the circuit simulations.

4. Conclusions

We have designed the high-speed BDD carry-save adders. By eliminating the feedback loop, the maximum frequency of the adder can be increased up to 38 GHz in the simulation. The high-speed adder was implemented by using the CONNECT cell library and the NEC Nb standard process, and its correct operation was confirmed at low and high speeds. The maximum frequency of adder was 23.8 GHz in the on-chip high-speed test.

Acknowledgments

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