Circuit/Device Modeling at the Quantum Level

Zhiping Yu, *Senior Member, IEEE*, Robert W. Dutton, *Fellow, IEEE*, and Richard A. Kiehl, *Fellow, IEEE*

***Abstract*—Quantum mechanical (QM) effects, which manifest when the device dimensions are comparable to the de Brogile wavelength, are becoming common physical phenomena in the current micro-/nano-meter technology era. While most novel devices take advantage of QM effects to achieve fast switching speed, miniature size, and extremely small power consumption, the mainstream CMOS devices (with the exception of EEPROMs) are generally suffering in performance from these effects. Solutions to minimize the adverse effects caused by QM while keeping the down scaling trend (technology feasibility aside) are being sought in the research community and industry-wide.**

This paper presents a perspective view of modeling approaches to quantum mechanical effects in solid-state devices at the device and circuit simulation levels. Specifically, the macroscopic modeling of silicon devices to include QM corrections in the classical transport framework is discussed. Both device and circuit models will be provided. On the quantum devices, such as the single electron junctions and transistors, the emphasis is placed on the principle of logic circuit operation.

***Index Terms*—Device and circuit simulation, MOS, quantum mechanical effects, single electron devices.**

I. Introduction

QUANTUM mechanical (QM) mechanisms have played a significant role primarily in compound semiconductor devices, such as resonant tunneling diode functioning as a switch and quantum well lasers for optoelectronic applications. However, due to the ever shrinking feature size of CMOS devices (toward tens nanometers in gate length), the QM effects manifest themselves even in the conventional silicon devices such as CMOS. In addition, small structures bring forth effects such as single electron tunneling, which might lead to new types of devices.

Since CMOS devices are ubiquitously used in digital and analog circuits, the circuit aspect of these QM effects has to be modeled properly. The operation of MOS devices is based on two fundamental aspects: 1) the channel charge induced by the gate at the surface of the substrate, capacitance–voltage (*C–V*) and 2) carrier transport from the source to drain along the channel, current–voltage (*I–V*). QM effects in the surface potential well have a profound impact on both the amount of charge which can be induced by the gate electrode through gate oxide and the profile of channel charge in the direction perpendicular to the surface (named transverse direction). The critical dimension in this direction is the gate oxide thickness, which now has fallen below 20 Å(2 nm) for the most advanced MOS devices. Another aspect which determines the device characteristics is the carrier transport along the channel (named lateral direction). Because of the two-dimensional (2-D) confinement of carriers in the channel, the mobility (or microscopically speaking the carrier scattering) would be different from the three-dimensional (3-D) scattering. Theoretically, the 2-D mobility would be higher than its 3-D counterpart because of less available energy states during the scattering (the 3-D energy band is split into 2D subbands in k-space due to QM effects). The transport issue is actually less critical in modeling for deep submicron devices since the carriers tend to traverse the channel with maximum speed (either saturation velocity or ballistically) for ultrashort ($<$100 nm) gate length at feasible power supply ($\sim$1 V). Yet another manifestation of QM effects is the tunneling phenomenon, which is the cornerstone for the operation of many quantum and conventional devices, such as single electron transistors and EEPROMs, and now starts to have severe impact on MOS operation as the gate oxide thickness keeps shrinking. To extract information accurately about the charge distribution alone requires the solution of Schrödinger and Poisson equations, assuming QM effects are to be fully accounted for. For most device applications, however, one-dimensional (1-D) solution is usually enough to reveal the critical information and to provide necessary corrections to the classical picture. Multidimensional (more than 1-D) solutions of Schrödinger and Poisson equations is difficult to obtain and in most cases is not necessary for prediction of device characteristics.

But from the circuit modeling point of view even 1-D solution of Schrödinger and Poisson equations is an overkill approach in term of both the complexity and computational cost. Analytical and macroscopic (in the sense of sticking to the classical transport framework by adding correction terms to account for the quantum mechanical effects) models would be preferable and could provide practical solutions. We term this type of solution approach as *QM corrections*.

In this article, QM corrections will be demonstrated in both the device and circuit modeling levels. The *C–V* simulation of MOS capacitors with gate oxide thickness of 30 Å and below will be used as examples. The discrepancy between the classical and QM corrected simulation can be as large as 20% compared to the measured data, while the QM correction method achieves practically the same result as does the more complete solution of Schrödinger and Poisson equations. Three models for the QM correction will be introduced: Hansch [1], van Dort [2], and hybrid [3] models. Then a more rigorous macroscopic transport model, the density gradient (DG) method, will be discussed. This model avoids *ad hoc* assumption to the material parameters or imposing an artificial shape function. The implementation

Manuscript received April 27, 2000. This work was supported by grants from DARPA (Contract DABT63-95-C-0090) and NSF (through NCCE Project ECS-9526378). The review of this paper was arranged by Editor M. Lundstrom.

Z. Yu and R. W. Dutton are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: yu@ee.stanford.edu).

R. A. Kiehl is with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN USA.

Publisher Item Identifier S 0018-9383(00)07786-8.

of the DG model using a script language approach will also be presented.

After describing the compact MOS model approach with QM corrections, the device and circuit models for logic circuits based on the single electron junctions will be discussed as the conclusion of this paper. In contrast to MOS models, these simulators are at a very early stage of development and use simple physical models describing only the most essential physics. Their importance is in providing tools to examine the basic feasibility of such new device and circuit concepts.

II. Correction Methods in QM Modeling of Silicon MOS Devices

As stated in the introduction section, the QM effects on MOS structures manifest mainly in two aspects: channel charge and carrier transport along the channel. We will only discuss the QM modeling of the channel charge in this section.

The channel charge is altered from its classical distribution by QM effects through two mechanisms: 1) The quantization of energy band to subbands in the surface potential well, effectively raises the ground energy level available for carrier to occupy in the surface region; 2) The carrier density distribution in the transverse direction is now determined by the superimposition of wavefunctions (eigenfunctions) at discrete energy levels (eigenvalues), both of which can be obtained from solving the Schrödinger equation in the surface potential well and applying the Fermi–Dirac statistics. Due to the repulsive boundary condition at the Si/SiO_2 interface (the barrier of SiO_2 to carriers in the substrate) to the wavefunctions, the resulting carrier profile peaks at a certain distance away from the interface in the surface quantum (i.e., potential) well.

The pioneer work in solving 1-D Schrödinger and Poisson equations in the transverse direction considering band structure was performed by Stern of IBM in late sixties and early seventies [4]. The key idea is to treat the channel carriers as a 2-D gas, and then the sheet carrier density (per unit surface area) can be determined by the (2-D) effective density of states (DOS) and the edge (i.e., bottom) of the subbands using normal Fermi–Dirac statistics. Since the 2-D DOS is a constant, independent of the energy, a simple expression for sheet carrier density, N, results in

$$N_i = N_{Ci} F_0\left(\frac{E_F - E_i}{kT}\right) \tag{1}$$

where $F_0(x) = \ln(1 + e^x)$ is the zero-order Fermi integral and the index i is for the energy valleys in the first Brillouin zone, and other symbols have conventional meanings. The energy levels for the bottom of (2-D) valleys are eigenvalues from solving the Schrödinger equation, together with the eigenfunctions, which represent the probability of carriers appear in a particular depth, z, in the transverse direction. Since the total carrier concentration is known over the entire z-axis (the sheet density for ith subband), the normalization of eigenfunction, $\zeta_i(z)$, is simply $\int_0^\infty \zeta_i^2(z)\,dz = 1$, and the carrier concentration at z would be

$$n(z) = \sum_i N_i \zeta_i^2(z). \tag{2}$$

This carrier density together with the ionized doping concentration contribute to the Poisson equation. The self-consistent solution of Schrödinger and Poisson equations will provide the carrier profile in the channel. This is essentially the manifestation of quantum effects in terms of gate-induced charge.

From the solution, there are two prominent features in the quantum mechanical picture compared to the classical results.

1) The channel carriers now are distributed among discrete eigenenergy levels instead of in a single energy band. The same Fermi–Dirac statistics applies to the sheet (2-D) instead of space (3D) carrier density.
2) The peak of the space carrier concentration is located some distance away from the surface in the substrate, which is a result of superimposition of wavefunctions at the different energy levels.

The above solution approach to QM effects, however, cannot easily be applied to multidimensional device simulation because of the difficulty in solving Schrödinger equation in multidimensional space, resulted from the delicacy in specifying the boundary condition for wavefunction. Even though the multidimensional Schrödinger equation can eventually be solved, the enormous computational effort and the limited benefit brought by such a solution do not justify it in practical applications.

Instead, researchers have been seeking approximate methods to incorporate QM effects in the classical physical framework by adding correction terms to the conventional transport models. We discuss here three analytical models used in the device simulation along this line of approach. All can be implemented in multidimensional device simulators.

The first such an analytical model was proposed by Hansch [1], which considers only the second aspect of the QM effects on charge distribution, that is, the repulsive boundary condition for channel carriers at the Si/SiO_2 interface. To satisfy this boundary condition, the Hansch model introduces a shape function which is to be imposed upon carrier concentration in the transverse direction. Effectively, the 3-D density of states (DOS) becomes a function of depth with near zero value at the surface:

$$N_C(z) = N_C\left[1 - e^{-(z+z_0)^2/\lambda^2}\right] \tag{3}$$

where z_0 is an offset to model the nonzero carrier concentration at the Si/SiO_2 interface due to the finite (i.e., noninfinite) oxide barrier height, λ is a characteristic length as a measure how fast the QM effects diminishes away from the interface. Note that except of the modification of the effective density of states, everything stays in the classical drift-diffusion picture. The current expression, however, now has to be changed accordingly to reflect the fact that N_C becomes position-dependent. This can be accomplished by explicitly evaluating symbolically the gradient of the quasi-Fermi level in the current expression, considering the position dependency of all relevant physical quantities.

$$\boldsymbol{j}_n = -q\mu_n n \nabla \phi_n. \tag{4}$$

The treatment is much like in dealing with heterostructure devices [5]. By using z_0 and λ as fitting parameters, device simulation incorporating the Hansch model gives correct carrier profile and can fit the *C–V* data with acceptable overall accuracy (Fig. 1). Still there are two shortcomings with this model. From

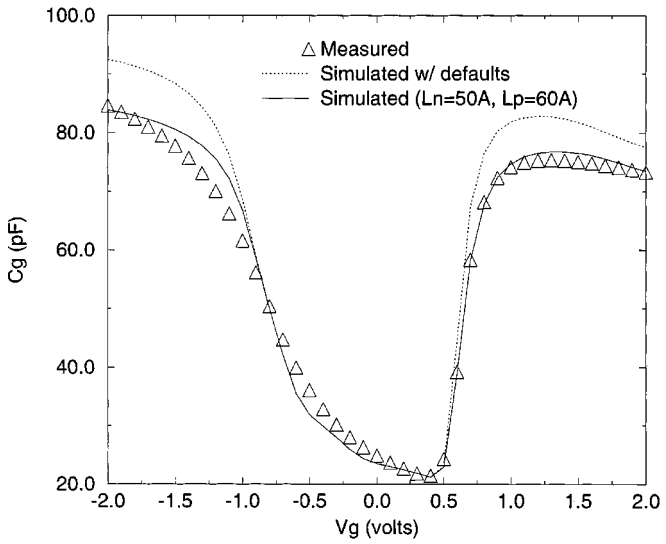

Fig. 1. Simulated *C–V* using Hansch's model compared to measured data for a MOS capacitor with gate oxide thickness of 31 Å. The optimized parameters are far from their default values and the trend in the accumulation region is not right.

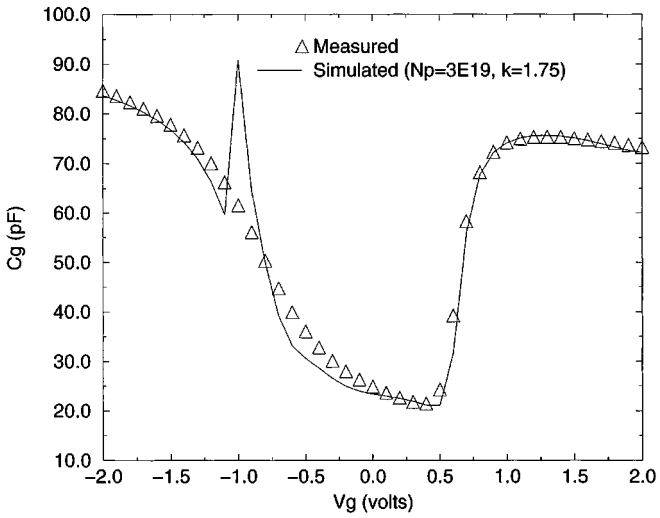

Fig. 2. Simulated *C–V* using van Dort model compared to measured data for a MOS capacitor with gate oxide thickness of 31 Å. The spike occurs at the flatband condition, i.e., $F_S = 0$.

a physical point of view, the characteristic length λ should be a function of the surface potential well which is predominantly characterized by the transverse surface electric field: the larger the electric field, the smaller the λ should be. But in the Hansch model, this dependence is lacking. The other shortcoming is that the Hansch model neglects the fact that the ground energy level is raised to above the band edge due to the energy quantization, which has a direct impact on the threshold voltage shift. Fig. 1 compares the simulation results with the measured data for an nMOS capacitor (p-substrate) with the gate oxide thickness of 31 Å using classical and Hansch models. It can be seen that the general agreement with the measured data by applying the Hansch model is good, but by using the default values for physical parameters in the model the discrepancy at the threshold voltage region, where the capacitance rapidly increases with the increase of the gate bias, is big and in the accumulation region the Hansch model fails to predict the continuous increase of the capacitance. To achieve a better simulation accuracy, the values for key parameters have to be adjusted from their physically meaningful default values.

The other model, proposed by van Dort [2], takes a different approach to including the QM effects. The model tries mainly to catch the fact of energy quantization, which effectively increases the bandgap at the surface region of the substrate under the gate. The amount of the bandgap increase is related to the surface transverse field. By solving the Schrödinger equation within a triangular potential well, one can find the relationship between the bandgap change with the transverse field. The modeling does not stop here, however. The van Dort model also includes the effect due to the repulsive boundary condition on the channel carriers, which is achieved by realizing that the distance of the peak in the channel carrier profile is related to the strength of the surface transverse field and their product can be considered as an additional increase in the bandgap. Through detailed analysis, it is found that both effects on the bandgap broadening (i.e., increase) are proportional to the 2/3 power of the surface transverse field, F_S. Considering the gradual decay of the bandgap broadening away from the surface, the following relation is used for modeling of bandgap increase:

$$\Delta E_g(z) = \beta F_S^{2/3} g(z) \tag{5}$$

where β is a physical constant and $g(z)$ is a decaying function [2]. Because the correction term, ΔE_g, is directly related to the applied bias through the surface field and the model captures two essential aspects of the quantum mechanical effects, the model works very well in simulating the *C–V* data as shown in Fig. 2.

Again there are problems with the van Dort model. First of all, by simply making the bandgap as the function of surface electric field and position (decay length), the profile of the channel carriers remains classical, that is, the carriers are peaked at the Si/SiO_2 interface. Second, it can be proved and intuitively determined as well that charge is proportional to the amount of the bandgap increasing, so it is proportional to $F_S^{2/3}$, implying that the gate capacitance which is the derivative of channel charge w.r.t. the gate bias, will suffer singularity at $F_S = 0$, the flatband condition.

To overcome these drawbacks, a hybrid model is proposed recently [3], which combines the Hansch and van Dort models by making the effective density of states the function of distance and at the same time by correlating the bandgap in the surface region with the surface transverse electric field. To eliminate the singularity of evaluating the capacitance at the flat band condition, $F_S = 0$, the following expression is used:

$$\Delta E_g \propto \frac{F_S^2}{ae^{-F_S^2/\sigma^2} + F_S^{4/3}}. \tag{6}$$

By adjusting the coefficients a and σ, the above expression has the same asymptotic behavior as the original one but no singularity at $F_S = 0$. A comparison is shown in Fig. 3.

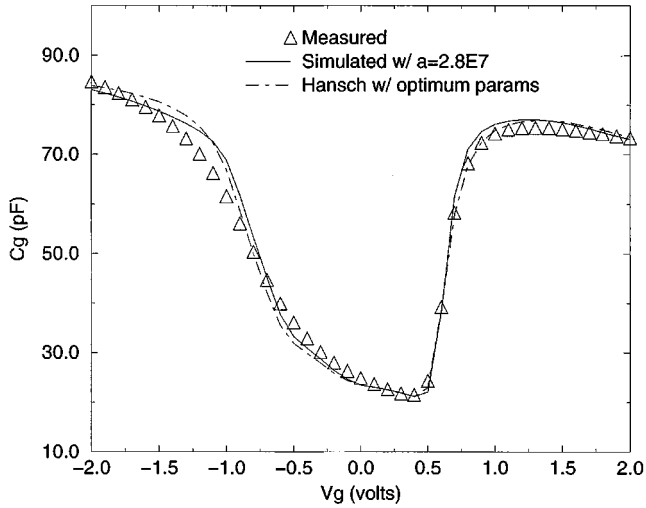

Fig. 3. Simulated *C–V* using hybrid model compared to measured data for a MOS capacitor with gate oxide thickness of 31 Å. The simulated *C–V* curve is not only smooth and all parameters are close to the physical ones.

III. Density Gradient Approach to QM Modeling

A more physics-based, yet still macroscopic, approach to incorporating the QM effects in classical transport model is the so-called density-gradient (DG) theory. The theory was developed based on the observation that the electron gas is energetically sensitive not only to its density but also to the gradient of the density. DG theory (or method) captures the nonlocality of quantum mechanics to the lowest-order (of $\hbar^2$) and can be derived directly from quantum mechanics [6]. From the macroscopic transport modeling point of view, DG theory essentially adds one additional term as the driving force, which is proportional to the gradient of a quantity which has something to do with the Laplacian of the square root of the carrier density, in the carrier flux (i.e., current density). Specifically, for electrons,

$$\boldsymbol{F}_n = n\mu_n \nabla\psi - D_n \nabla n + 2nb\mu_n \nabla\left(\frac{\nabla^2\sqrt{n}}{\sqrt{n}}\right) \tag{7}$$

where the third term on the right-hand side of the equation accounts for the quantum corrections, which can also be considered to lump with the first term and constitutes the so-called quantum potential, and the coefficient b has the dependence of

$$b = \frac{\hbar^2}{12 m_n^* q} \tag{8}$$

The DG formulation can be used to model both the carrier confinement (and repulsive boundary condition) and tunneling in an MOS system.

There is an implementation issue involving the DG model, i.e., there will be fourth order derivative term on n in the carrier continuity equation due to the quantum correction term as compared to only the second-order derivative for the conventional drift-diffusion model. The difficulty in discretization caused by higher order derivative can be alleviated by introducing additional variables and equations to the physical system. A new concept and platform for solving a system of PDEs representing a physical system in semiconductor process and device simulation have recently been developed jointly at Bell Laboratories and Stanford. The first serious application of this program, called PROPHET, in device simulation is the implementation of the above DG model. The new physical system with five variables was quickly assembled (i.e., prototyped) by users at the script language level and has been applied to the analysis of the same MOS capacitor problem as discussed above. The results are very promising both in terms of the accuracy and physical meaningfulness. A detailed discussion of this computational experiment is provided in [8].

IV. Compact Model to MOS Devices

The above approaches are mainly useful in the device simulation level. In the circuit analysis even such complexity is not acceptable. Hence, there are several compact models available for incorporating the QM effects in the circuit simulation.

The first approach is to use the effective oxide thickness instead of the physical one. A simple formula based on detailed quantum mechanical analysis gives the following expression for the effective oxide thickness [7]:

$$t_{ox,\,\mathrm{eff}} = t_{ox} + \alpha\left(Q_b + \tfrac{11}{32} Q_i\right)^{-1/3} \tag{9}$$

where $\alpha = 3.5 \times 10^{-10}$ $(C$ cm$)^{1/3}$, and Q_b and Q_i are the bulk and inversion layer charges per unit area, respectively. As an example, for the physical gate oxide thickness of 68 Å, to achieve a reasonable fit to the measured *C–V*, the effective (or called electrical) oxide thickness would be 79 Å [10].

The other approach resembles more the van Dort model used in the device simulation. Essentially, the surface potential, ϕ_s, in a compact MOS model (say, BSIM 3v3), is calculated from the QM-corrected intrinsic carrier concentration, n_i^{QM}, as follows:

$$n_i^{\mathrm{QM}} = n_i^{CL} e^{(\Delta E_g/2kT)} \tag{10}$$

and ΔE_g results from the van Dort's bandgap broadening model

$$\Delta E_g = \frac{13}{9}\beta\left(\frac{\epsilon_{Si}}{4kT}\right)^{1/3} F_S^{2/3} \tag{11}$$

where $\beta = 4.1 \times 10^{-8}$ eV-cm and in the compact model the transverse surface field can either be calculated based on the charge in the substrate (the sum of inversion and depletion charges in the channel region and below) or be approximated using $F_S = (V_{GS} + V_{th})/(6t_{ox})$ for nMOS [9]. All the symbols above have conventional meaning except of those explained explicitly. The calculation results by using the above model for a 0.35 μm CMOS process agrees well with both the measured *C–V* data and simulated *I–V* from the device simulation [10].

V. Compact Model for Other QM Devices: Single Electron Tunneling Devices

As we have just discussed, highly scaled CMOS devices become sensitive to the quantum mechanical wave nature of electrons. We now turn our attention to a case that is based on a quantum mechanical tunneling process and where the discreteness of electrons plays an essential role. This is the case of Coulomb blockade or single electron tunneling effect.

Single electron effects [11] are the basis of a number of proposals for radically new types of logic and memory circuitry and are important in conventional devices such as flash memories when scaled to ultra small dimensions. When an electron tunnels through a junction with a capacitance C that is so small that the Coulomb energy associated with a single electronic charge $E_c = q^2/(2C)$ is large compared with other energies in the system, a number of potentially useful effects occur. For example, when biased by a dc current I, a single junction exhibits coherent oscillations at a frequency $f = I/q$. The oscillations occur due to the interplay between the quasicontinuous charging of the junction and the discrete tunneling of electrons. Effectively, the discrete tunneling is blocked until the junction voltage reaches a level where the free energy of the system (the Coulomb energy) is reduced by the tunneling event. As a result, the junction behaves like an ultrasmall oscillator in which a single electron tunnels each ac cycle. This provides the basis for a logic approach in which the logic states are related to the electrical phase of the oscillation, called "tunneling phase logic" [12], as will be described later. If two ultrasmall junctions are connected in series and the common node is coupled to a gate electrode, this same interplay of quasicontinuous charging and discrete tunneling leads to a dc electrical characteristic somewhat similar to that of a conventional MOSFET. Current is blocked for certain ranges in the gate bias and flows for other ranges, thereby providing a gate controlled switch. Logic approaches reminiscent of CMOS have been proposed for such devices, called "single electron transistors" [13], as discussed later. A variety of other types of electronic circuitry, including logic circuits in which the logic state is represented by the presence or absence of a single electron on a particular tunneling junction [14], [15] and memories based on the storage of a single electron (or a few electrons) on a small island have also been proposed [16].

Most models of single electron devices are based on a simple theory referred to as the "orthodox" theory [17]. A basic assumption of the orthodox theory is that the resistance R of the tunnel barriers in the system is much greater than the quantum unit of resistance R_Q. This means that the tunnel barriers have low-transparency, thereby insuring that the electron is localized within a particular conducting island at any instant of time. The electron tunneling time through the barrier is also ignored within the orthodox theory. Furthermore, electron energy quantization within the small conductive islands forming the tunnel junctions is not taken into account. Thus the commonly used models based on the orthodox theory of single electron tunneling are really semiclassical, with much of the quantum mechanical nature left out. The models focus on the statistical nature of the tunneling process as influenced by changes in the electrostatic energy in the system.

The tunneling of an electron through a barrier is a random event and occurs at a rate Γ that depends on the resulting reduction the free (electrostatic) energy ΔW of the system. Within the orthodox theory

$$\Gamma(\Delta W) = \frac{1}{q} I(\Delta W/q) \frac{1}{1 - e^{-\Delta W/(kT)}} \tag{12}$$

$$\Delta W = q(V_i - V_t) \tag{13}$$

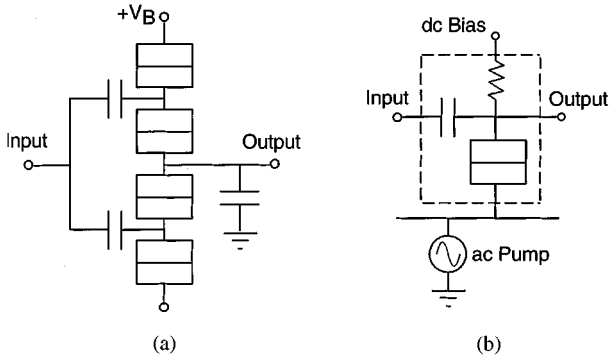

Fig. 4. (a) Basic CSET inverter gate for single electron transistor logic. (b) Basic TPL inverter gate for single electron tunneling phase logic.

and

$$V_t \equiv q(C^{-1})_{kl} - \frac{q}{2}\left[(C^{-1})_{kk} + (C^{-1})_{ll}\right] \tag{14}$$

where

V_i voltage drop across the barrier before the tunneling event;
C^{-1} reciprocal capacitance matrix of the system;
k and l label the islands on either side of the barrier.

Simulation of the random dynamics of single electron systems can be done by using a Monte Carlo method to determine the "actual" tunneling event once the rates Γ for all the junctions are known. Monte Carlo simulators have been developed by the various groups working in the field and several simulators, including MOSES[1] and SIMON,[2] are readily available.

The Monte Carlo method models the underlying microscopic physics of the system and thus provides not only average quantities needed to determine dc device characteristics but also the tunneling dynamics needed in the study of circuit operation. In addition, this method allows complex systems to be simulated in reasonable computing times. However, Monte Carlo techniques are not useful for including such effects as co-tunneling, a quantum mechanical effect in which several events occur at the same time. In this case the "master" equation method has been used. In this method, the time evolution of the probability of each state p_i is found by solving the system of equations

$$\frac{dp_i}{dt} = \sum_j (\Gamma_{j\to i}\, p_j - \Gamma_{i\to j}\, p_i). \tag{15}$$

The master equation method has been incorporated into the programs SIMON and SETTRANS (see footnote 1). The usefulness of the master equation approach is limited, however, to simple systems having only a few tunnel junctions. Also, since this approach deals only with averages, it is not useful for investigating the dynamics of the microscopic tunneling events in single electron circuits.

Fig. 4 shows examples of two types of single electron circuits to which the modeling techniques described above have

[1]Program developed by workers at the State University of New York and available via anonymous ftp from the site hana.physics.sunysb.edu/pub/

[2]Program developed by workers at the Institute for Microelectronics, Technical University of Vienna, and available through website http://members.magnet.st/catsmeow/

been applied. Fig. 4(a) shows the basic inverter gate of CSET logic, a logic scheme that resembles CMOS technology. This approach is based on generating dc *I–V* characteristics similar to FET's by exploiting the single electron tunneling effect in pairs of series-connected junctions (single electron transistors), as mentioned above. The dc input voltage changes the background electrostatic potentials of the gate electrodes, thereby changing the distribution of the bias voltage $2V_B$. Circuits that exploit both the positive and negative transconductance characteristics in single electron transistors to produce complementary (CMOS-like) operation have also been proposed [18]. The Monte Carlo and master equation methods have been used extensively in the analysis of such circuits [19]. Fig. 4(b) shows the basic inverter gate of tunneling phase logic (TPL) [20]. TPL is based on the phase locking of single electron tunneling oscillations to an ac pump signal that is distributed throughout the circuit. Because the pump frequency is set to twice the tunneling frequency, the electrical phase of the locked oscillation can take on two different values, each representing a logic state. Monte Carlo simulations have been used to study the statistical properties of TPL [20] and the basic logic operation of TPL devices, including the operation of multiple-valued TPL gates [21].

The experience thus far is that models based on the orthodox theory of single electron tunneling have provided good agreement with many experiments, especially those for metallic systems where quantum mechanical size effects are relatively small (compared with semiconductors). These models have also been useful in exploring the basic operation of various device and circuit proposals. However, since the E_c must be much greater than kT for useful operation of the circuits proposed thus far, physical structures must be scaled to extremely small dimensions around 1 nm if practical operating temperatures are to be reached. At these dimensions (small clusters of atoms), it will no longer be possible to neglect quantum size effects even in metallic systems. As circuit simulations reach large numbers of devices and statistical error rates become a more central issue, effective methods for incorporating effects such as co-tunneling will also be important. Thus the development of accurate compact models will eventually become as important for single electron approaches as they presently are for CMOS.

VI. Conclusions

Device and circuit models of solid-state devices including CMOS and "quantum" devices (e.g., SET for single electron transistors) are selectively reviewed. It is important to realize that in the micro-/nano-technology era, quantum mechanical (QM) effects have become principal or first order ones in device operation, for good or bad. Although, all QM effects should be able to be explained and modeled to required accuracy by solving the Schrödinger equation with other semiconductor equations, for practical applications only those models which maintain the macroscopic formulation while incorporating the QM effects as *correction* terms, will be accepted by circuit and device designers. To make those macroscopic (or analytical) models applicable to a broad range of devices and their operation ranges, however, underlining physics have to be preserved as much as possible.

Acknowledgment

The authors express gratitude to the following people for providing experimental data and intriguing discussion: P. Vande Voorde (HP Laboratories, HP), M. G. Ancona (Naval Research Laboratories), C. S. Rafferty (Bell Laboratories, Lucent Technologies).

References

[1] W. Hänsch, T. Vogelsang, R. Kircher, and M. Orlowski, "Carrier transport near the Si/SiO_2 interface of a MOSFET," *Solid-State Electron.*, vol. 32, p. 839, 1989.

[2] M. J. van Dort, P. H. Woerlee, and A. J. Walker, "A simple model for quantization effects in heavily-doped silicon MOSFET's at inversion conditions," *Solid-State Electron.*, vol. 37, p. 411, 1994.

[3] C.-H. Choi, Z. Yu, and R. W. Dutton, "Modeling of MOS scaling with emphasis on gate tunneling and source/drain resistance," Superlattices Microstruct., vol. 27, p. 191, 2000, to be published.

[4] F. Stern, "Self-consistent results for n-type Si inversion layers," *Phys. Rev.*, vol. 5, p. 4891, June 1972.

[5] Z. Yu and R. W. Dutton, "SEDAN III—A generalized electronic material device analysis program,", Stanford, CA, Tech. Rep., July 1985.

[6] M. G. Ancona and H. F. Tiersten, "Macroscopic physics of the silicon inversion layer," *Phys. Rev. B*, vol. 35, p. 7959, 1987.

[7] F. Stern, "Quantum properties of surface space-charge layers," *CRC Crit. Rev. Solid State Sci.*, pp. 499–514, 1974.

[8] C. S. Rafferty *et al.*, "Multi-dimensional quantum effect simulation using a density-gradient model and script-level programming techniques," in *SISPAD'98*, Lueven, Belgium, Sept. 1998, p. 137.

[9] K. Chen, H. C. Wann, P. K. Ko, and C. Hu, "The impact of device scaling and power supply change on CMOS gate performance," *IEEE Electron Device Lett.*, vol. 17, no. 5, p. 202, May 1996.

[10] R. Rios *et al.*, "A physical compact MOSFET, including quantum mechanical effects, for statistical circuit design applications," in *IEDM Tech. Dig.*, 1995, p. 937.

[11] H. Grabert and M. H. Devoret, *Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures*, ser. Series B: Physics. New York: Plenum, 1992, vol. 294.

[12] T. Ohshima and R. A. Kiehl, "Operation of bistable phase-locked single-electron tunneling logic elements," *J. Appl. Phys.*, vol. 80, pp. 912–923, 1996.

[13] K. K. Likharev, "Single electron transistors: Electrostatic analogs of DC SQUIDS," *IEEE Trans. Magn.*, vol. MAG-23, p. 1142, 1987.

[14] D. D. Averin and K. K. Likharev, *Possible Applications of the Single Charge Tunneling*. New York: Plenum, 1992.

[15] M. G. Ancona, "Design of computationally useful single-electron digital circuits," *J. Appl. Phys.*, vol. 79, pp. 526–539, 1996.

[16] K. Yano *et al.*, "Room-temperature single-electron memory using fine-grain polycrystalline silicon," in *IEDM Tech. Dig.*, 1993, pp. 541–545.

[17] D. V. Averin and K. K. Likharev, "Single electronics: A correlated transfer of single electrons and Cooper pairs in systems of small tunnel junctions," in *Mesoscopic Phenomena in Solids*, B. L. Altshuler, P. A. Lee, and R. A. Webb, Eds. New York: Elsevier, 1991, pp. 173–271.

[18] J. R. Tucker, "Complementary digital logic based on "Coulomb blockade"," *J. Appl. Phys.*, vol. 72, p. 4399, 1992.

[19] R. H. Chen, A.N. Korotkov, and K. K. Likharev, "Single-electron transistor logic," *Appl. Phys. Lett.*, vol. 68, pp. 1954–1956, 1996.

[20] T. Ohshima, "Stability of binary logic tunneling phase states in dc-biased and ac-pumped single-electron tunnel junctions," *Appl. Phys. Lett.*, vol. 69, pp. 4059–4061, 1996.

[21] F. Y. Liu, F.-T. An, and R. A. Kiehl, "Ternary single electron tunneling phase logic element," *Appl. Phys. Lett.*, vol. 74, pp. 4040–4042, June 28, 1999.

[22] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev.B*, vol. 39, pp. 9536–9540, May 1989.

Zhiping Yu (M'90–SM'90) received the B.S. degree from Tsinghua University, Beijing, China, in 1967, and the M.S. and Ph.D degrees from Stanford University, Stanford, CA, in 1980 and 1985, respectively.

He is currently a Senior Research Scientist in the Department of Electrical Engineering, Stanford University, and also holds a Full Professorship at Tsinghua University. His research interests focus on IC process, device, and circuit simulation, and in particular, the numerical techniques and modeling of RF and heterostructure devices. He has been involved in efforts to develop a simulation package for optoelectronic devices and 3-D solid modeling for ICs. Besides the full time university research, he is a Consultant to HP Computer System and Technology Lab, HP, developing advanced transport models for subquarter-micron CMOS technology, including quantum mechanical effects.

Dr. Yu is currently serves as the Associate Editor of IEEE TRANS. COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, responsible for TCAD-related fields.

Robert W. Dutton (S'67–M'70–SM'80–F'84) received the B.S., M.S., and Ph.D. degrees from the University of California, Berkeley, in 1966, 1967, and 1970, respectively.

He is Professor of Electrical Engineering at Stanford University and Director of Research in the Center for Integrated systems. He has held Summer staff positions at Fairchild, Bell Telephone Laboratories, Hewlett-Packard, IBM Research, and Matsushita during 1967, 1973, 1975, 1977, and 1988, respectively. His research interests focus on IC process, device, and circuit technologies—especially the use of CAD and parallel computational methods. He has published more than 200 journal articles and graduated more than four dozen doctorate students.

Dr. Dutton was Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (1984–1986). He was awarded the 1987 IEEE J. J. Ebers Award, a 1988 Guggenheim Fellowship to study in Japan, was elected to the National Academy of Engineering in 1991, and received the Jack A Morton Award for 1996.

Richard A. Kiehl (F'97) received the B.S., M.S., and Ph. D. degrees from the School of Electrical Engineering, Purdue University, West Lafayette, IN.

From 1974 to 1980, he was a Member of Technical Staff at Sandia National Laboratories, where he initiated studies of microwave semiconductor devices. In 1980 he joined AT&Bell Laboratories, Murray Hill, NJ, as a Member of Technical Staff. He was a leading contributor to the Bell Lab's research on heterostructure devices and circuits, particularly heterostructure field-effect transistors. He joined IBM T. J. Watson Research Center in 1985 as Research Staff Member and focused his work on heterostructure-based CMOS circuitry in III-V compound and SiGe heterostructure materials. In 1993, he became Assistant Director of the Quantum Electron Device Laboratory, Fujitsu Laboratories Ltd, Atsugi, Japan, where he lead research on nanoelectronic circuitry. He was on the faculty at Stanford University, Stanford, CA, from 1996 to 1999 as Acting Professor in the Department of Electrical Engineering. He began his present position as professor of Electrical and Computer Engineering, University of Minnesota, Minneapolis, in 1999. His current research is focused on electronic devices and circuitry based on new physical concepts in novel nanometer-scale structures and on the exploration of the interface between nanotechnology and biotechnology for electronic applications. He is co-editor of *High Speed Heterostructure Devices*.

Prof. Kiehl has served as Associate Editor of IEEE ELECTRON DEVICE LETTERS.