A Multiple-Valued SRAM with Combined Single-Electron and MOS Transistors

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We report here a new type of "single-electron" memory that works as a multiple-valued SRAM. A schematic of the proposed memory is shown in Fig. 1. The source of a MOSFET with fixed gate bias V_{gg} is connected to the drain of a single-electron transistor (SET), and the SET drain voltage is kept nearly constant around V_{gg}-V_{th}, where V_{th} is the threshold voltage of the MOSFET. This V_{gg}-V_{th} is set low enough to sustain the Coulomb-blockade condition. By connecting the SET gate to the MOSFET drain, the I_d-V_{gs} (3-terminal) characteristics of the SET are converted to the I-V (2-terminal) characteristics of the combined SET-MOSFET circuit. With a proper choice of load device, the periodic nature of the I-V characteristics results in a number of stability points, and this realizes the multiple-valued memory operation.

The SET is fabricated by pattern-dependent oxidation (PADOX) [*], in which a one-dimensional Si wire patterned in silicon on insulator (SOI) is converted into a small Si island with a small tunnel capacitor at each end. Figure 2 shows the I_d-V_{gs} characteristics of a SET. Periodic drain-current peaks are clearly seen along with an effect of tunnel resistance modulation by the gate voltage. From this figure and a Coulomb diamond plot, gate capacitance, source/drain capacitance, and tunnel resistance are calculated to be 0.3 aF, 2.7 aF, and 80~220 kΩ, respectively.

PADOX is highly compatible with CMOS fabrication process since the area other than one-dimensional Si wire can be used as an ordinary MOSFET channel. Figure 3 shows the I_d-V_{gs} characteristics of a MOSFET on the same SOI wafer. The effective channel width, length, and gate oxide thickness are 12 μm, 14 μm, and 90 nm, respectively. The requirements for the present application, such as small off-state leakage and steep subthreshold slope, are met by this MOSFET.

Figure 4 shows the I-V characteristics of the combined SET-MOSFET circuit. The current increases and decreases periodically, reflecting the I_d-V_{gs} characteristics of the SET (Fig. 2). If a current source of 4.5 nA is connected to the circuit, stability points **a**~**f** should appear. Note that the number of stability points is infinite in principle, but is practically limited by the breakdown voltage of the MOSFET drain or SET gate and the deviation from the ideal SET characteristics.

The multiple-valued memory operation was verified by current sweep measurements. If the current starts from stability point **a** and increases, the voltage jumps up when the current exceeds the second peak in the I-V characteristics (Fig. 4). If the current sweep is reversed at this moment, stability point **b** can be reached. Other stability points, **c**~**e**, can also be reached by choosing higher current-sweep reversal points. Note that stability point **f** cannot be attained by this current-mode operation, because the last peak in the I-V characteristics (Fig. 4) is lower than the previous one.

Figure 6 proposes a four-transistor memory cell for large-scale applications. A depletion-mode grounded-gate MOSFET **M1** is used to sustain the SET drain voltage around the absolute threshold voltage of **M1**. Another depletion-mode MOSFET, **M2,** with its gate and source shorted serves as a current source, and pass-transistor **M3** controls the access to the cell. In write operation, the voltage applied to **BL** is transferred through **M3**, and is quantized to a stability point after **M3** is cut off. It should be noted that any stability point can be directly reached by this voltage-mode operation.

In summary, we have devised a novel multiple-valued SRAM comprised of a SET and a MOSFET, and the basic operation is verified with devices fabricated on the same SOI wafer. The result opens up the possibility of dramatically increasing the memory density of future scaled-down CMOS.

[*] Y. Takahashi et al., IEEE Trans. Electron Devices, Vol. 43, pp. 1213-1217, 1996.

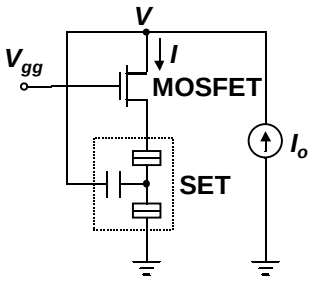

Fig. 1 The proposed multiple-valued static memory comprised of a SET, a MOSFET and a constant-current source I_o. By connecting the SET gate to the MOSFET drain, the I_d-V_{gs} (3-terminal) characteristics of the SET are converted to the I-V (2-terminal) characteristics.

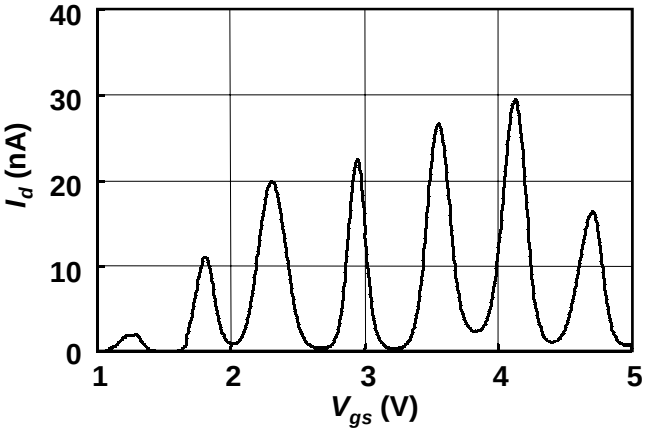

Fig. 2 I_d-V_{gs} (3-terminal) characteristics of a SET fabricated by PADOX, measured at 27 K and 10 mV of V_{ds}.

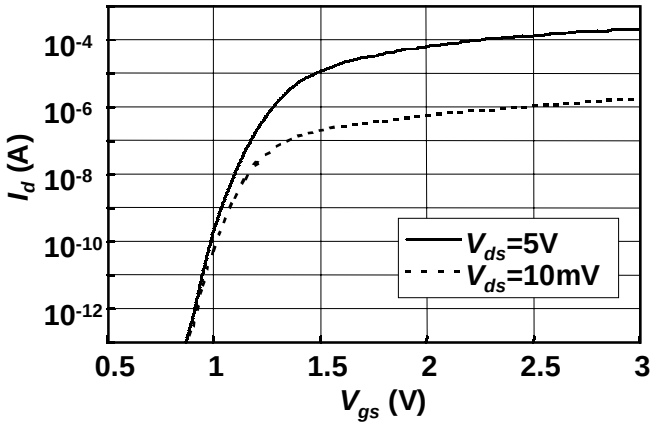

Fig. 3 I_d-V_{gs} (3-terminal) characteristics of a MOSFET fabricated on the same SOI wafer for the above SET, measured at 27 K.

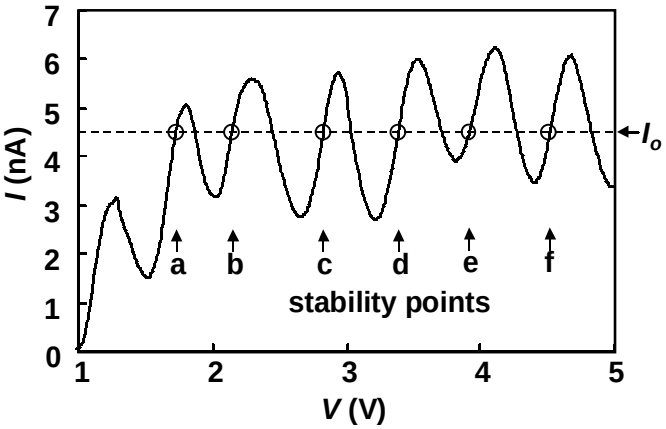

Fig. 4 I-V (2-terminal) characteristics of the proposed circuit measured at 1.08 V of V_{gg}. Stability points (**a**~**f**) expected for the current load of 4.5 nA are also shown.

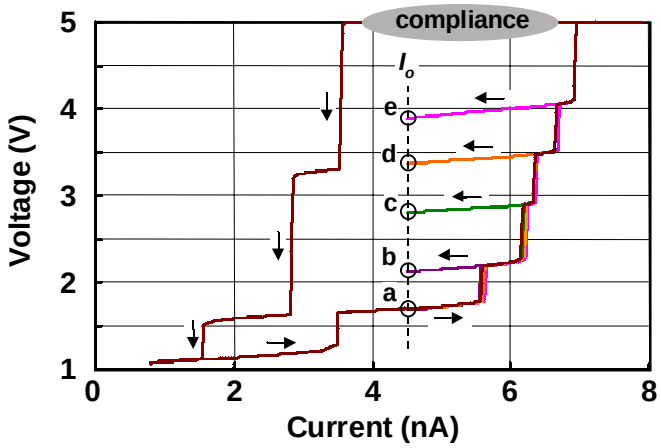

Fig. 5 Current sweep measurements of the proposed circuit. The compliance of the current source is 5 V.

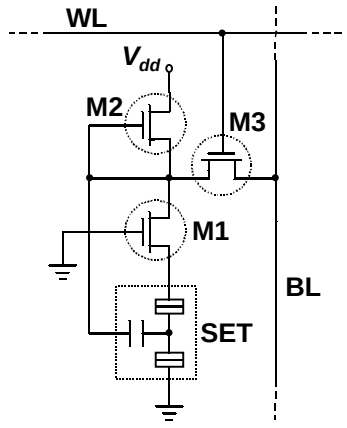

Fig. 6 A multiple-valued "single-electron" SRAM cell with two depletion-mode MOSFETs (**M1** and **M2**) and one enhancement-mode MOSFET (**M3**).