SET Logic

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Abstract

Single-electron tunneling transistors can manipulate individual electrons. These device dissipate little power and can be fabricated in sizes ranging down to a molecular scale. It has been suggested that large scale integration of single-electron transistors could result in logic circuits with a high device packing density. Recently, a number of different logic schemes using single-electron tunneling transistors have been proposed. A brief overview of these developments is presented here.

Single-electron tunneling (SET) devices can monitor and manipulate the motion of individual electrons.[1-3] The small size and low power dissipation of SET circuits makes them potentially useful for the information technology industry. In the first SET logic scheme proposed by Likharev and Averin, bits were represented by individual electrons.[1] This logic (called single-electron logic) has an architecture similar to superconducting single flux quantum logic where individual magnetic flux quanta are manipulated.[4] Ancona also proposed a logic scheme where bits were represented by individual electrons but he proposed building circuits with a regular cellular structure and with local connections as in a cellular automata.[5] Tucker[6] and Yoshikawa[7] et al. suggested the use of single-electron tunneling transistors in an architecture very similar to CMOS. In this case the bits are represented by voltage levels.[8,9] Figure 1 shows two CMOS-like inverters constructed from SET transistors. Tougaw and Lent suggested that the electron configuration in a cluster of quantum dots could be used to encode the information.[10] The clusters of quantum dots are placed very close together but they are not electrically connected. The information passes from one cluster to the next via the Coulomb interaction between the electrons. Computation proceeds locally as in a cellular automata architecture. Korotkov proposed a similar computational scheme using clusters not connected by wires.[11] Unlike Tougaw and Lent, Korotkov suggested the use of an ac driving field so that the energy needed to drive the computation could be coupled into each of the clusters directly. Ohshima and Kiehl also proposed a SET logic scheme using an ac pump (tunneling phase logic).[12] In this scheme the information is not coded in the configuration of some charge on a cluster but it is coded in the relative phase between the ac pump and the periodic single-electron tunneling oscillations. Likharev and Korotkov proposed reversible logic elements[13] where the amount of energy dissipate per switching event could be much less than $k_B T$. There have also been several suggestions to use single-electron tunneling transistors to build neural nets. Goossens et al. suggested exploiting the periodic transfer characteristics of a SET transistor to build neural nets[14] while the quantum neuromorphic networks of Bandyopadhyay et al.[15] function more like a traditional Hopfield machine.

Although many logic schemes have been proposed, no logic family has been thoroughly characterized experimentally. One of the problems is that it has been difficult to fabricate complex circuits with the very small feature sizes necessary (< 100 nm) for single electronics circuits. In order for SET circuits to function, the energy that is necessary to add an electron to a device must be larger than the characteristic thermal energy $k_B T$. If this is not the case, the single-electron effects will be washed out by thermal fluctuations. In order to make the electron addition energy (also called the charging energy) large, the capacitance of the devices must be made so small that e^2/C is much larger than $k_B T$, where C is the capacitance of the device. This requires that the dimensions of the devices be very small. Presently, complex SET circuits are made with critical dimensions of about 50 nm.[16] At this scale, the circuits are still not very reliable and only work at low temperature. There are many reports of individual SET transistors that work at room temperature but those fabrication technologies do not allow wires to cross and no room temperature transistors with voltage gain have been produced. These two conditions are necessary for making
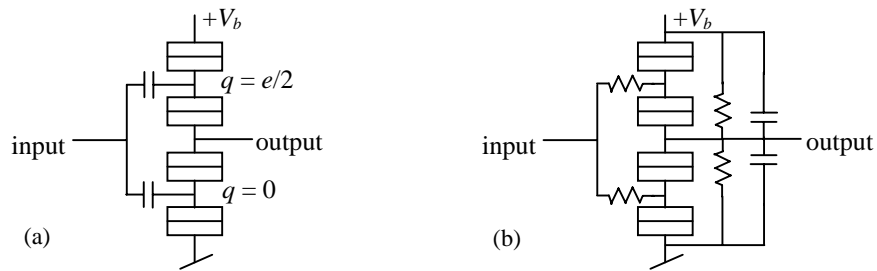
FIGURE 1. (a) A SET inverter realized with capacitively coupled SET transistors. The offset charges q are specified to insure proper inverter operation. (b) A SET inverter realized with resistively coupled SET transistors.

complex logic circuits. Recently there has been considerable progress in fabricating smaller devices. It is likely that complex molecular-scale devices will be fabricated reasonably soon. When that happens SET circuits will operate at room temperatures.

Another problem that SET circuits face is the presence of offset charges.[17] Offset charges are charged defects in or near SET circuits. They can be interstitial atoms or charged vacancies which can polarize a SET transistor with a charge that is a fraction of an electron. SET circuits are extremely sensitive to charge; the operation of many circuits is completely disrupted by the presence of the offset charges. Most of the logic schemes described above simply will not work if the offset charges are not somehow eliminated. The prospects for eliminating the offset charges seem rather small. It is therefore important to focus on logic schemes such as the resistively coupled SET transistor logic of Yoshikawa et al.[7] which is offset-charge independent.

The future role that SET devices will have in general purpose computation remains unclear. The large scale realization of SET circuits that function at room temperature will have to wait for advances in fabrication technology that will allow for the mass production of molecular scale devices. No SET logic scheme is presently threatening to overthrow the semiconductor industry standard CMOS technology. However, different schemes are continuously being proposed and one of these may prove to be superior in some ways to mainstream semiconductor devices. In any case, miniaturization will likely remain an important aspect of dense integrated circuits and single electron effects will almost certainly play a role in devices with very small dimensions.

Acknowledgments

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