A Multiple-Valued Logic with Merged Single-Electron and MOS Transistors

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Abstract

We propose merged single-electron and MOS devices that serve as basic components of multiple-valued logic, such as a universal literal gate and a quantizer. We verified their operation by using single-electron transistors and MOSFETs fabricated on the same wafer by pattern-dependent oxidation process. We also discuss their application to an analog-to-digital converter and a multiple-valued adder.

Introduction

Multiple-valued logics (MVLs) have potential advantages over binary logics with respect to the number of elements per function and operating speed (1-4). They are also expected to relax the interconnection complexity on the inside and outside of integrated circuits (2). Most MVL circuits have been fabricated with conventional transistors like MOSFETs (1,2) and bipolar transistors (3), or with negative-resistance devices represented by resonant tunneling diodes (4). However, their success has been limited, partially because the devices are inherently single-threshold or single-peak, and are not fully suited for MVL. In this sense, it is more natural to utilize the emerging single-electron devices (5,6) because the discreteness of electronic charge in a Coulomb island can be directly related to multiple-valued operation. Actually some single-electron MVL circuits have been proposed (7,8), but the operation has not yet been verified experimentally mainly because their schemes require unrealistic accuracy or limitations of device parameters and operating conditions. In this paper, we introduce a type of MVL circuit consisting of single-electron transistors (SETs) and MOSFETs for practical application. We demonstrate the operation of the basic components of MVL, such as a universal literal gate and a quantizer, using devices fabricated by the Si-based pattern-dependent oxidation (PADOX) process (9,10). The usefulness of the proposed single-electron MVL is discussed using an analog-to-digital converter (ADC) and a multiple-valued adder as examples.

Principle of Operation

Fig. 1(a) shows a schematic of the universal literal gate comprising a SET and a MOSFET. A MOSFET with a fixed gate bias of V_{gg} is used here to keep the SET drain voltage almost constant at V_{gg}-V_{th}, where V_{th} is the MOSFET threshold voltage. This results in the I_d-V_{in} characteristics being independent of V_{out} [Fig. 1(b)], and sharp square-wave-like input-output characteristics with a large voltage swing [Fig. 1(c)]. Conventional SET inverters could not attain such characteristics because the voltage gain of a discrete SET is usually very small, and the applicable voltage is limited to sustain the Coulomb blockade condition.

Figure 2(a) shows a schematic of the proposed quantizer. Periodic I_d-V_{gs} characteristics of a SET can be converted to 2-terminal I_d-V_{out} characteristics when the SET gate and the MOSFET drain are shorted [Fig. 2(b)]. With a constant-current load I_o, many stability points appear, and V_{in} fed through the transfer-gate MOSFET is quantized to a stability point after the gate is cut off. This results in the V_{in}-V_{out} characteristics shown in Fig. 2(c).

Note that the number of periods in the universal literal characteristics [Fig. 1(c)] or voltage levels in the quantizer characteristics [Fig. 2(c)] is infinite in principle. This is a unique feature of the proposed SET-based MVLs, and leads to a considerable reduction of the number of devices in a circuit.

Experiments

Both the SET and the MOSFET were fabricated on a thin silicon-on-insulator (SOI) layer. A possible layout and the corresponding circuit diagram of the integrated SET and MOSFET are shown in Figs. 3(a) and (b). The SET is created in a narrow wire region by PADOX (9,10). The quantum size effect raises the potential in the wire, but in the middle of the wire the high compressive stress generated by the oxidation reduces the bandgap [Fig. 3(c)] (10). This creates two tunnel barriers and an island sandwiched between them, which constitute a SET. Since the areas outside the wire can easily be used for MOSFETs, PADOX is highly compatible with the CMOS process.

Fig. 4 shows the I_d-V_{gs} characteristics of a SET. Periodic drain-current peaks are clearly seen along with the effect of tunnel resistance modulation by the gate voltage. From this figure and a Coulomb diamond plot, gate capacitance C_g, source/drain capacitance C_s/C_d, and tunnel resistance were calculated to be 0.27 aF, 2.7 aF, and 80~220 kΩ, respectively. The maximum voltage gain of the discrete SET (C_g/C_d) is as small as 0.1, but this presents no problem in constructing the merged SET-MOSFET device.

Fig. 5 shows the subthreshold characteristics of a MOSFET fabricated on the same SOI wafer for drain voltages of 5 V

and 10 mV. The gate length, width and the gate oxide thickness are 14 μm, 12 μm and 90 nm, respectively. The device exhibits good cutoff and a small shift due to the drain voltage, which are suitable for the proposed applications.

Fig. 6 shows the input-output characteristics of the proposed literal gate. When the SET I_d-V_{gs} curve corresponding to the V_{ds} assigned by the V_{gg} setting crosses the load line I_o, the output switches between high and low levels as is seen in Fig. 6. The swing is sharp, and the amplitude of the swing is as high as 5 volts.

Fig. 7 shows the 2-terminal I_d-V_{out} characteristics of the SET-MOSFET device with the SET gate shorted to the MOSFET drain. The current increases and decreases periodically, reflecting the I_d-V_{gs} characteristics of the discrete SET. If we connect a current source of 4.5 nA, stability points **a**~**f** corresponding to quantized levels should appear.

Quantizer operation is verified with the setup shown in Fig. 8. The transfer-gate MOSFET1 and MOSFET2 for probing are connected externally. A triangular wave is fed to V_{in}, and the gate of MOSFET1 is driven by short pulses of ***CLK***. The waveforms are shown in Fig. 9. V_{out} is quantized to levels **a**~**f** that correspond to stability points in Fig. 7. Operation speed shown in the figure is not limited by the intrinsic performance of the device, but by the large stray capacitance of 370 pF existing at V_{out}.

Discussions

Fig. 10 proposes a block diagram of a 3-bit flash ADC. Whereas a conventional n-bit flash ADC requires n^2-1 components such as comparators, the SET ADC (11,12) requires only n components. In addition, this particular ADC with a quantizer at the front end and the SET-MOSFET literal gates does not require comparators, latches, or ramp generators at each literal gate. The use of Gray code is not necessary either, since the quantizer prevents the entry of intermediate voltage levels.

Fig. 11 is a circuit diagram to realize the ADC in Fig. 10. The circuit is remarkably simple. For example, the main blocks except for the quantizer require only 9 transistors and 5 capacitors, which is half the 28 transistors required for a conventional implementation (1).

Fig. 12 shows the block diagram of a full adder for redundant positive-digit number representation PD2-3 (1). The main parts of this adder are the same as that of the 3-bit ADC in Figs. 10 and 11. Thus, the number of elements can be reduced to a half by the use of the merged SET-MOSFET devices. In addition, this multiple-valued arithmetic itself has the merit of high-speed operation due to the elimination of carry propagation.

Conclusions

By combining a SET with a MOSFET, we made the best use of the periodic nature of the SET characteristics and obtained a universal literal gate with sharp transfer characteristics and large output amplitude. We also verified the operation of a novel quantizer based on the same scheme. These basic components for MVL are extremely compact in that the former requires only three elements and the latter only four. Moreover, the number of periods or quantized levels is infinite in principle and does not affect the circuit size. With these components, we showed that a 3-bit flash ADC and a carry-propagation-free adder for redundant number representation PD2-3 could be made with half the number of elements in a conventional implementation. The results open up the possibility of constructing a new class of MVL with single-electron devices.

Acknowledgments

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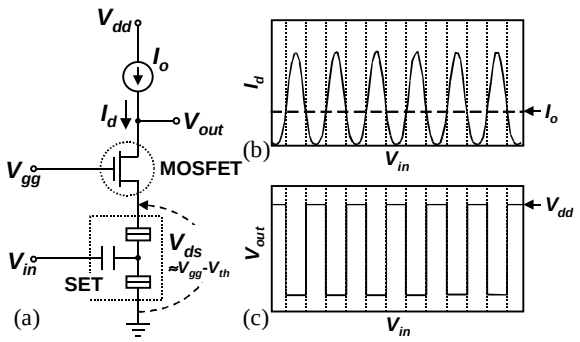

Fig. 1 (a) A schematic of the universal literal gate comprising a SET and a MOSFET. (b) I_d-V_{in} characteristics, which are almost completely independent of V_{out} since the V_{ds} of the SET is kept nearly constant at V_{gg} minus V_{th}, the threshold voltage of the MOSFET. (c) Expected transfer (V_{in}-V_{out}) characteristics.

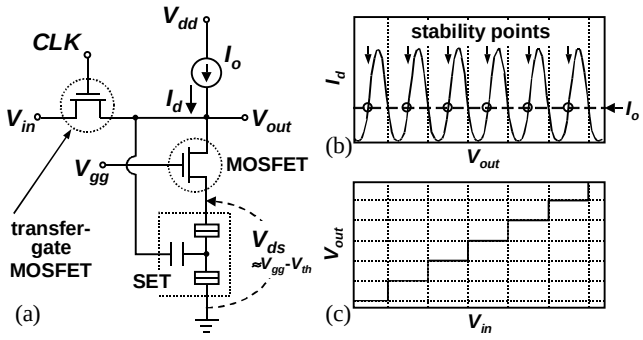

Fig. 2 (a) A schematic of the proposed quantizer. (b) 2-terminal I_d-V_{out} characteristics of the merged SET-MOSFET device with the SET gate shorted to the MOSFET drain. (c) Expected transfer (V_{in}-V_{out}) characteristics. V_{in} is transferred to V_{out} through the transfer gate MOSFET, and is quantized to a stability point after the gate is cut off.

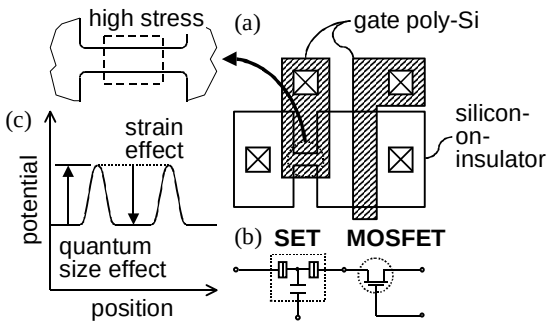

Fig. 3 (a) A possible layout of the integrated SET and MOSFET. (b) Circuit diagram corresponding to the layout above. (c) Potential profile along the length of the narrow wire where a SET is created by the pattern-dependent oxidation (PADOX) (9,10). Since areas outside the wire can readily be used for MOSFETs, PADOX is highly compatible with a CMOS process.

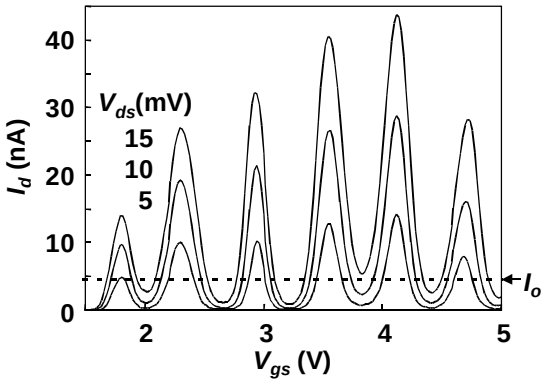

Fig. 4 I_d-V_{gs} characteristics of a SET fabricated by the PADOX process, measured at 27 K. From this figure and a Coulomb diamond plot, gate capacitance C_g, source/drain capacitance C_s/C_d and tunneling resistance are calculated to be 0.27 aF, 2.7 aF and 80~220 kΩ, respectively.

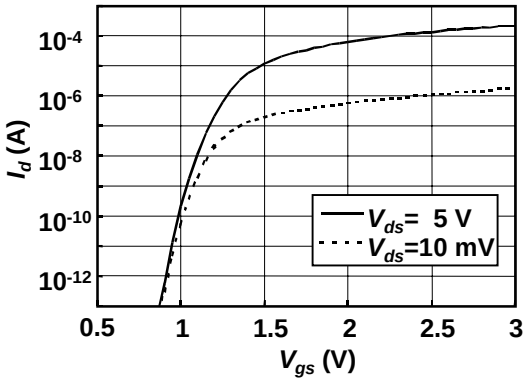

Fig. 5 I_d-V_{gs} characteristics of a MOSFET fabricated on the same SOI wafer as the above SET, measured at 27 K. Effective channel width, length and gate oxide thickness are 12 μm, 14 μm and 90 nm, respectively. Threshold voltage V_{th}, corresponding to I_d=4.5 nA and V_{ds}=3 V, is 1.07 V, and transconductance G_m at V_{ds}=V_{gs}=3 V is 151 μS.

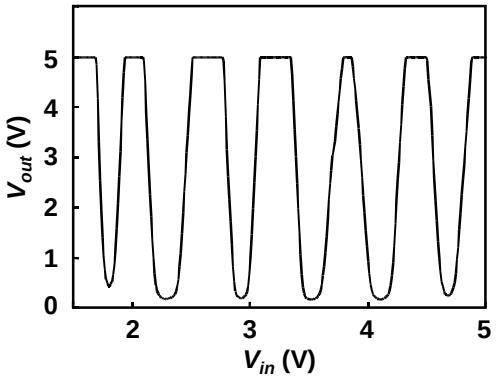

Fig. 6 Measured transfer (V_{in}-V_{out}) characteristics of the proposed literal gate comprising a SET and a MOSFET [Fig. 1(a)] with V_{gg} of 1.08 V and a current load of 4.5 nA. Originally, the SET I_d-V_{gs} characteristics have a large V_{ds} dependence as indicated in Fig. 4, and this V_{ds} dependence is alleviated by the MOSFET, resulting in a large voltage swing and sharp rises and falls.

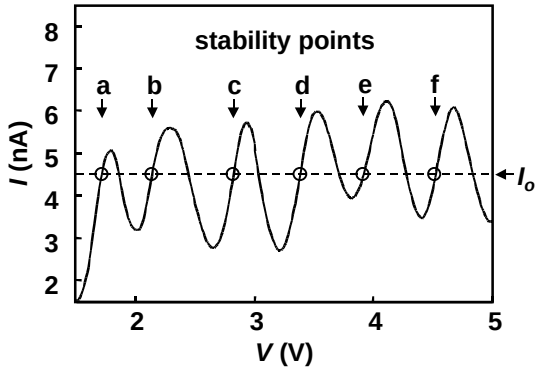

Fig. 7 2-terminal I_d-V_{out} characteristics of the merged SET-MOSFET device with the SET gate shorted to the MOSFET drain, measured at 1.08 V of V_{gg}. Stability points (**a**~**f**) expected for the current load of 4.5 nA are also shown.

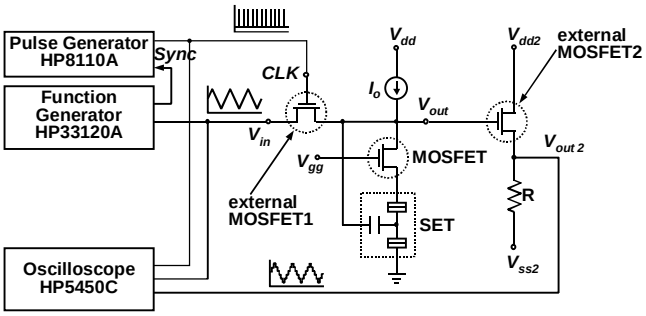

Fig. 8 Measurement setup for the quantizer proposed in Fig. 2(a). The external MOSFET2 is used as an FET probe to measure the V_{out} sustained by a small current (~nA).

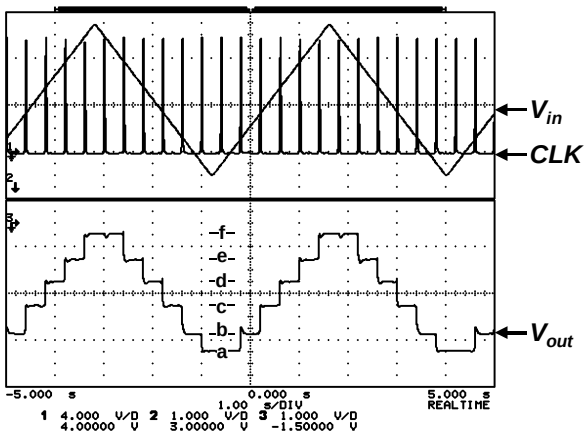

Fig. 9 Quantizer operation measured by the setup in Fig. 8, with V_{gg} of 1.08 V and a current load of 4.5 nA. Operation speed is not limited by the intrinsic performance of the device, but by the large stray capacitance of 370 pF existing at V_{out}.

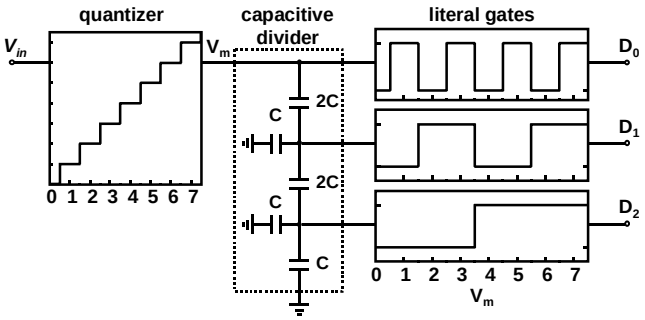

Fig. 10 A block diagram of a 3-bit flash ADC. A conventional ***n***-bit flash ADC requires n^2-1 components, whereas the SET ADC (11,12) requires only ***n***. In addition, this particular ADC with a quantizer at the front end and with the SET-MOSFET literal gates does not require comparators, latches or ramp generator at each literal gate. The use of Gray code is not necessary either.

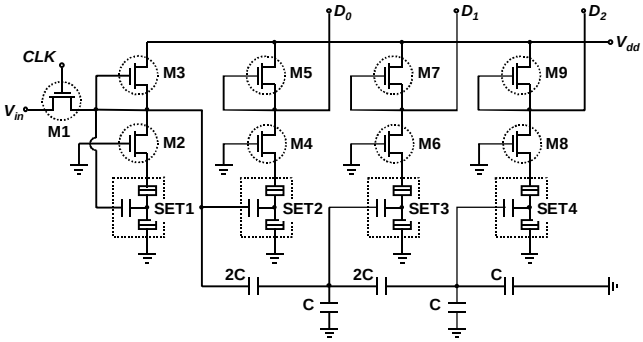

Fig. 11 A circuit diagram of the 3-bit ADC in Fig. 10. Depletion-mode MOSFETs, M2, 4, 6 and 8, keep the drain voltage of the SETs nearly constant at the absolute threshold voltage, and other depletion-mode MOSFETs, M3, 5, 7 and 9, serve as current sources.

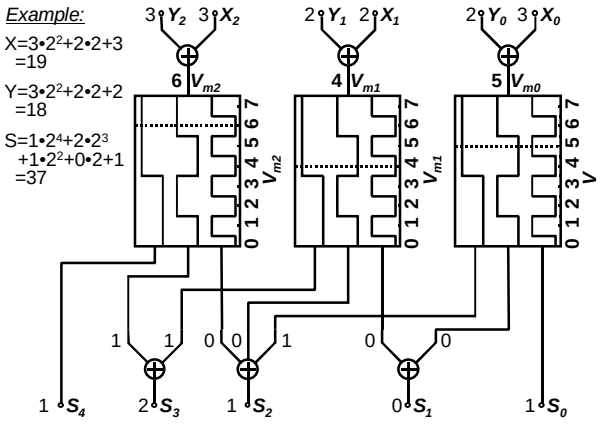

Fig. 12 A full adder for redundant positive-digit number representation PD2-3 (1) consisting of three ADC blocks without a quantizer and linear sums (⊕). This is free from carry propagation, and is thus high-speed. By using the merged SET-MOSFET devices, multiple-valued logics of this kind can be made with half the number of elements in conventional implementation.