Silicon Single-Electron Devices and Their Applications

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Abstract

We have developed two novel methods of fabricating very small Si single-electron transistors (SETs), called PAttern-Dependent OXidation (PADOX) and Vertical PAttern-Dependent OXidation (V-PADOX). These methods exploit special phenomena that occur when small Si structures on SiO_2 are thermally oxidized. Since the size of the resultant Si island of the SET is about 10 nm, we can observe the conductance oscillations in the SET even at room temperature. The controllability and reproducibility of these methods are excellent because of the stability of the thermal oxidation process. We are using PADOX and V-PADOX to integrate single-electron devices (SEDs) for sophisticated functions. We have fabricated and tested several kinds of memory and logic devices. This paper also describes applications of multi-input gate SETs to multiple-valued logic circuits.

1. Introduction

Recent advances in deep-submicron CMOS technologies have made it possible to load a small Si chip with an enormous number of transistors. However, the power consumption of the chip monotonicaly increases as the number of transistors increases. This will limit the integration scale because the power consumption will exceed the cooling limit. The single-electron transistor (SET) is expected to be a key device for future extremely large-scale integrated circuits because of its ultrtalow power consumption and small size. The SET has a great potential for low-power yet high-performance signal processing and hence for furthering the multimedia society.

The most difficult aspect in fabricating SETs is how to sandwich a nanometer-scale island between two small tunnel capacitors. We have already developed two sophisticated patterning methods, called PADOX (PAttern-Dependent OXidation) [1-2] and V-PADOX (Vertical PAttern-Dependent OXidation) [3], to make such structures. In these methods, special phenomena that occur during oxidation of Si nano-structures on SiO_2 play a crucial role. The size of the Si-island formed by these methods is about 10 nm, which is small enough to observe conductance oscillations in the SET even at room temperature. Section **2** briefly outlines the operation principles of SETs. The fabrication methods are presented in section **3**. These methods have great flexibility for fabricating various types of single-electron devices. Section **4** presents two kinds of memory devices that were developed by applying PADOX. Applications to logic circuits are described in section **5**. In addition, we describe new applications of multi-input gate SETs to multiple-valued logic circuits.

2. Single-Electron Transistor (SET)

The SET is the most fundamental of the various single-electron devices (SEDs) [4, 5]. Simple three-terminal operation of the device [6, 7] was first verified experimentally in a metal-insulator system in 1987 [8, 9]. The SET must have a small conductive island to exploit the Coulomb blockade for manipulating electrons by means of one-by-one transfer. Figure 1 shows an equivalent circuit of a SET. The total capacitance C_{total} of the SET island limits the highest operating temperature of the device because the single-electron charging energy of the island $e^2/2C_{\text{total}}$ has to be much larger than the thermal energy kT, where e is the elementary charge, k is the Boltzmann constant and T is absolute temperature. If we impose the condition for operation [10]

$$e^2/2C_{\text{total}} > 3.5kT\,, \qquad (1)$$

the C_{total} should be smaller than 0.88 aF ($0.88\text{x}10^{-18}$F) for room temperature (kT = 25.9 meV) operation. When the island is a sphere with a radius of r embedded in a dielectric material with a dielectric constant of ε, the self capacitance Cs is given by

$$C\text{s} = 4\pi\varepsilon\varepsilon_0\, r\,. \qquad (2)$$

The self capacitance gives the minimum value of the capacitance of the island, since this is the capacitance when the counter electrode is at infinite distance. The radius of the sphere must be smaller than 8 nm to realize a capacitance of 0.88 aF even if the dielectric constant of the surrounding material is unity. Therefore, a nanometer-scale fabrication process is critical in producing islands for high-temperature operation.

Typical electrical characteristics of a single-electron transistor fabricated by PADOX are shown in Fig. 2. The source-drain conductance exhibits oscillatory characteristics as a function of gate voltage. At the valleys, the conductance is suppressed due to the Coulomb blockade. As a result, the number of electrons stored in the SET island is a fixed integer l. When the gate voltage, which can control the potential of the island, increases to a certain value at which conductance shows a peak, the chemical potential of the two

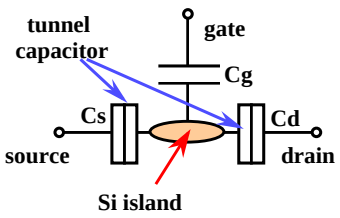


Fig. 1. Equivalent circuit of a SET.

states, one for l electrons and the other for l+1 electrons becomes equal, which means that the island can contain l or l+1 electrons. Therefore, if a small voltage is applied between the source and drain electrodes, electrons flow one at a time. The number of the electrons in the island is l+1 after one electron tunnels from the source to the island. This number returns to l after an electron tunnels from the island to the drain. By repeating this sequence, a current due to single-electron tunneling flows at the conductance peaks.

Conductance oscillations due to the Coulomb blockade in a semiconductor island were first observed at about 0.4 K in a double-gated Si MOSFET by Scott-Thomas et al. [11] These characteristics originated in small islands that had unintentionally been formed in a narrow one-dimensional wire. This result stimulated investigation of small semiconductor dots formed by the use of lithography [10]. Until recently, however, the operating temperature of SETs has been limited to below 4 K because of the difficulties in fabricating an SET island whose capacitance is of the order of 1 aF. In particular, the islands of SETs became unavoidably larger than the minimum feature size of the lithography. Therefore the formation of nanometer-scale islands requires the development of new fabrication methods.

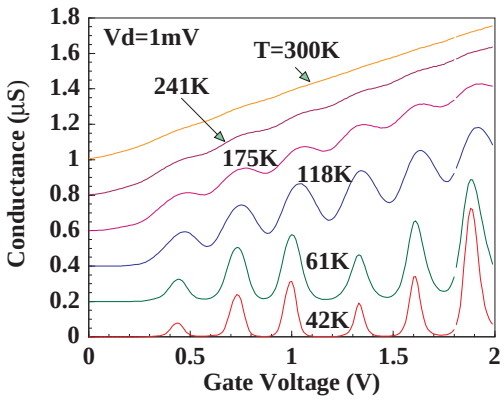


Fig. 2. Typical conductance oscillations of a SET fabricated by PADOX as a function of the gate voltage measured at various temperatures and at a drain voltage of 10 mV.

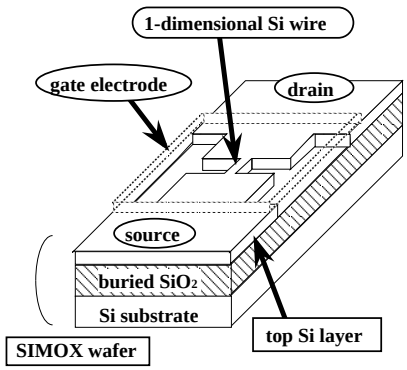


Fig. 3. Initial device structure of the SET. We used a SIMOX (Separation by IMplanted OXygen) wafer, which is a type of SOI wafer. The small 1-dimensional Si wire is converted to a small Si island. The Si island is surrounded by the gate electrode, substrate Si, and source and drain electrodes.

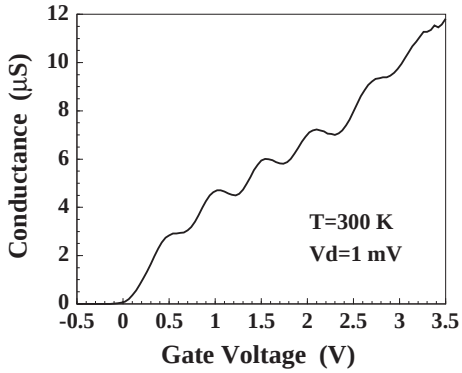


Fig. 4. Conductance oscillations as a function of the gate voltage measured at 300 K (room temperature) and at a drain voltage of 10 mV. Initial wire width, length and height were all 30 nm.

Any kinds of conductive material can be used to fabricate a SET. Metals and III-V compound semiconductors have so far been studied from the physical point of view, such as Cooper pair tunneling of small superconducting metal Josephson junctions and coherent or ballistic tunneling in compound semiconductors with high mobility. However, silicon is the most promising material for application to LSIs because SETs made of Si can be used jointly with conventional CMOS circuits. In addition, advanced fabrication technologies for sub-quarter-micron CMOS LSIs can be used to make small Si structures. We tried to exploit these features in order to fabricate SETs with nanometer-scale Si islands, which can be operated at temperatures near 300 K.

3. Novel Fabrication Methods (PADOX and V-PADOX)

3.1. PADOX (Pattern-Dependent Oxidation)

Thermal oxidation of Si is accepted as being the simplest and most controllable process in Si LSI technology. However, it is well known that complicated oxidation occurs in small Si structures because of the mechanical stress that builds up in the newly-formed oxide [12, 13]. We realized that a small Si pattern could be converted into a small SET when we observed that the amount of oxidation at particular point can be modulated in a way that depends on the initial pattern. This is the reason why we call this method PAttern-Dependent OXidation (PADOX) [1, 2]. The structure fabricated on a thin SOI (Silicon On Insulator) wafer contains a narrow and short Si wire as shown in Fig. 3. PADOX converts the wire into a small island with a small tunnel capacitor at each end. The basic mechanism of this conversion is that the oxidation in the middle of the wire is suppressed due to stress accumulated during thermal oxidation while oxidation at the ends of the wire is enhanced due to both the supply of oxygen from the back and less accumulation of stress. The constrictions formed at both ends of the wire function as tunnel barriers. The SET is completed by forming a poly-Si gate over the island region, as shown in Fig. 3. The advantages of this method are that an island smaller than the initially defined size can be made and that tunnel barriers are automatically formed at both ends of the wire.

The characteristics of a SET fabricated by PADOX (Fig. 4) indicate that the total capacitance of the SET island is as small as 1 aF [1, 2, 14-16]. In addition, the device has a relatively low tunnel resistance, from several hundred kΩ to several MΩ [1, 14]. This is advantageous for high-speed operation. For example, if a load capacitance of about 20 aF, which comes from the next-stage gate and wiring, is assumed, the expected delay time is about 10 ps. Another advantage is that the fabrication process is very stable and reproducible [15, 16] because it is almost the same as the conventional Si process. This should make it possible to use SETs in combination with MOSFETs [16, 17].

Using this method, we have been investigating the integration of single-electron devices (SEDs) to create new functions. Several kinds of devices, such as memory and logic devices, have been fabricated and their fundamental operations have been confirmed. Fabrication of these devices was performed by applying PADOX to appropriately designed patterns. We also added ultrafine poly-crystalline Si gates to some of them by using electron-beam lithography. Detailed description of these devices are given in section **4** and **5**.

3.2. V-PADOX (Vertical Pattern-Dependent Oxidation)

We have also developed an alternative pattern-dependent oxidation method that can form *twin* SET islands. As shown in Fig. 5(a), the initial structure has a fine trench in the middle of a Si wire. Oxidation converts the edge regions of the thin Si layer under the trench into two small islands of about the same size; these islands are embedded in SiO_2 and are connected to the initially thicker Si layers by tunnel barriers that are formed automatically during oxidation. Figures 6(a) and (b) show cross-sectional TEM images of a thick and a thin Si wire, respectively. At both edges of the thin Si layer, small Si islands are formed in a self-aligned manner and the rest of the thin region is converted into SiO_2. This is because stress accumulation causes less oxidation to occur around the edges. It is noteworthy that the two tiny Si islands are formed without the need for lithographic definition of the islands themselves. As a result, two SETs connected in parallel to each other can be obtained by forming a gate electrode over the islands. Since the starting pattern of Si is vertically modulated, we call this method V-PADOX [3]. The equivalent circuit of the device is shown in Fig. 5(b).

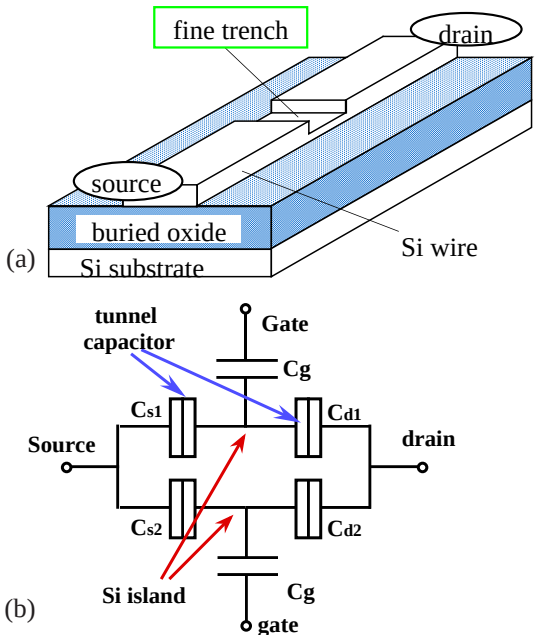


Fig. 5. Initial structure of the twin SETs before V-PADOX (a) and the equivalent circuit of the device (b). *W*, *L*, *d* represent the designed wire width, trench length, and trench depth, respectively.

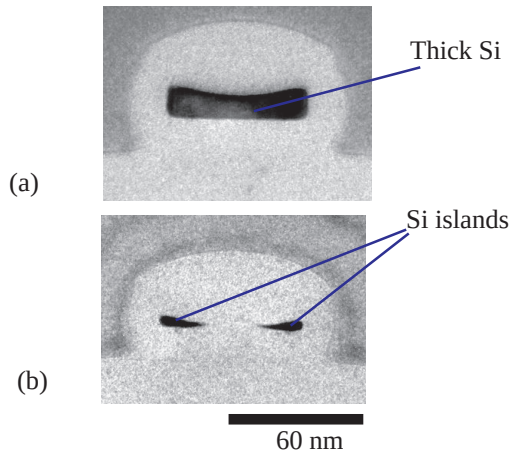


Fig. 6. Cross-sectional TEM image of the Si wire after V-PADOX. Initial thicknesses of the wire were 22 nm (a) and 14 nm (b). Wire width is 60 nm. Small Si islands are

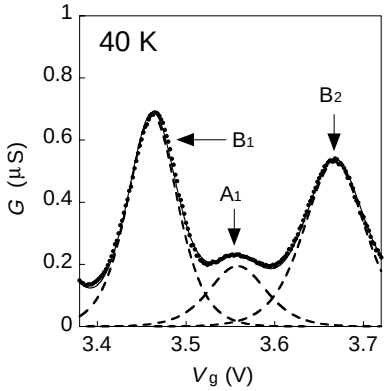


Fig. 7. Conductance oscillations of a twin-island SET as a function of the gate voltage measured at 40 K and at a drain voltage of 10 mV. Dots are measured data while the solid line is the curve derived from fitting analyses. The broken lines, A and B, indicate the individual conductance of each SET.

Figure 7 shows the gate voltage dependence of the conductance, measured at 40 K with a drain voltage of 10 mV, for a twin-island SET with a trench length *L* of 30 nm and a wire width *W* of 80 nm. The measured conductance oscillation can be deconvoluted into two oscillations, denoted as A

and B in the figure. It was demonstrated that each oscillation can be independently controlled by the voltage applied to the side gates (not shown in Fig. 7), which were placed at each side of the trench. This fact indicates that each SET operates independently. This method can produce two small SETs at the same time in a tiny area, which is of great advantage to the construction of the integrated logic circuits [3] described in section **5**.

4. Memory Devices Fabricated by Using PADOX

4.1. Memory device in combination with MOSFET

The most fundamental application of SETs is as memory devices. One example fabricated by using PADOX is a novel memory device that requires only a small number of electrons [16, 17]. Figure 8(a) shows a SEM (Scanning Electron Microscopy) image of such a device fabricated on a thin SOI wafer. The equivalent circuit is shown in Fig. 8(b). The device has a small Si memory node at the tip of the 1-dimensional Si wire. A fine gate electrode overlaid on the wire forms a small MOSFET, which controls the flow of electrons into and out of the memory node. The other 1-dimensional wire is connected to the source and the drain electrodes and forms the SET, which detects the small number of electrons stored in the memory node. Figure 9 shows the hysteresis characteristics of the SET current during "write" and "store" operations measured at 40 K. The gate voltage V_{lg} of the 1-dimensional MOSFET was initially set to a low voltage of -2.7 V, at which the channel of the 1-dimensional MOSFET was closed. The side-electrode voltage V_{se} was changed from 0 to -1 V, and the gate voltage V_{lg} was scanned up to -2.1 V and then backed down. The rapid fall in the SET current around V_{lg} = -2.3 V, the voltage at which the MOSFET turned on, indicates a flow of electrons into the memory node. After the downward scan, the SET current does not return to the initial level because the memory node already contains excess electrons. The number of stored electrons is about 100. Since the SET is sensitive to a very small amount of charge, this memory device can operate with only a small number of electrons. This result clearly shows that PADOX-fabricated devices can be used in combination with conventional MOSFETs.

4.2. Single-electron memory

Another type of memory device can be created by applying PADOX to the Si pattern shown in Fig. 10(a). PADOX converts each branch of the cross-shaped bridge region between the two wide Si layers into a Si island; two of the four islands serve as SET islands, and the others serve as single-electron memory nodes [18]. A simplified equivalent circuit of the device is illustrated in Fig. 10(b). The device has different conductance oscillation curves depending on the number of electrons stored in the satellite island, because the extra electrons in the island shift the curve in the higher gate-voltage direction. The inset of Fig. 11 shows the hysteresis characteristics of the conductance measured at 40 K. The gate voltage was scanned several times forward and backward, and the data were plotted on the same graph. The conductance curves are split into three oscillation curves. In addition, there are some jumps in the conductance from one curve to another. The time-resolved measurement of the jumps shown in Fig. 11 clearly indicates the abrupt transition in the conductance, which suggests the single-electron tunneling between the SET island and satellite islands. These phenomena can be exploited for a memory device operating with a single electron.

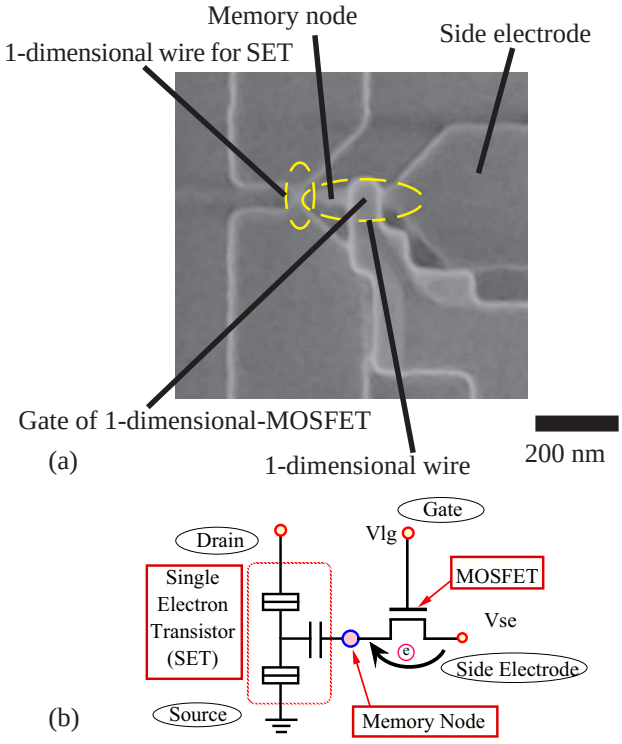


Fig. 8. SEM image of a fabricated memory device (a) and its simplified equivalent circuit (b).

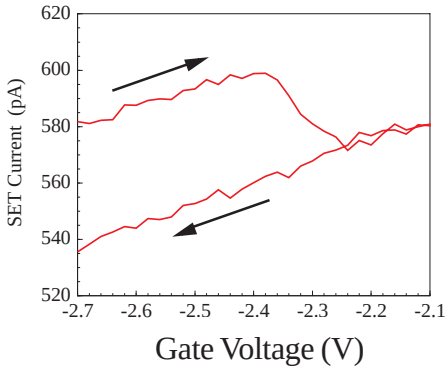


Fig. 9. Hysteresis characteristics of SET current representing "write" and "storage" actions measured at 40 K. The gate voltage V_{lg} scan started just after the V_{se}, initially 0 V, was set at -1 V.

5. Logic Circuits

5.1. CMOS-type logic circuit

One of the most prominent features of SETs is their low-power operation capability. This strongly suggests that the devices could be used in logic circuits. It will be favorable

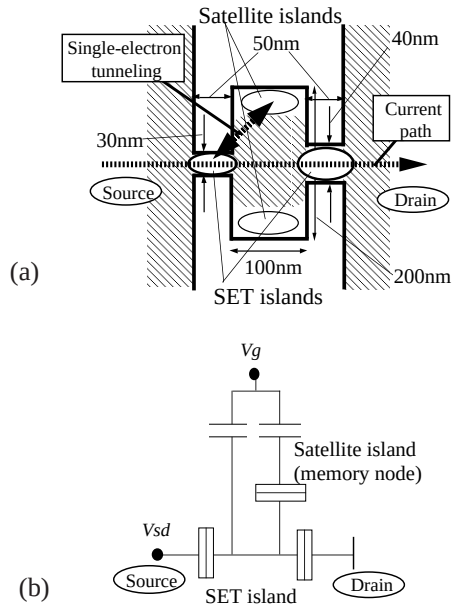


Fig. 10. Schematic structure of cross-shaped bridge region (a) and simplified equivalent circuit (b). The hatched region indicates the cross-shaped Si bridge and source and drain regions. After PADOX, Si islands, shown as ovals, are formed.

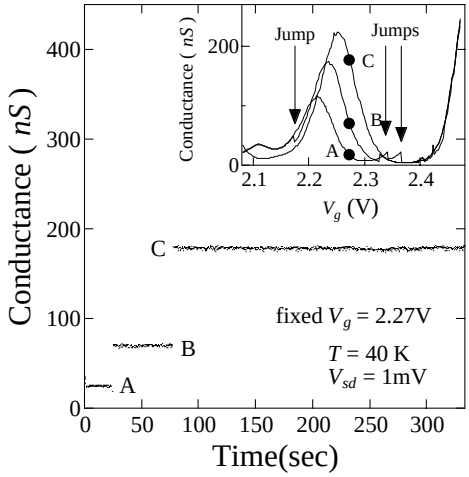


Fig. 11. Conductance as a function of time measured at 40 K and at a drain voltage of 1 mV after the gate voltage is applied at 2.27 V. The inset shows three conductance curves reflecting the single-electron memory effect measured by scanning the gate voltage forward and backward several times. Arrows indicate the jumps in

if we could construct single-electron logic circuits in which SETs operate analogously to MOSFETs in CMOS (or NMOS) logic circuits [7, 19], because it would allow us to utilize the sophisticated circuit design technology of the current generation of LSIs. We fabricated a complementary single-electron inverter, a circuit element for single-electron CMOS-type logic circuits, as a first step of this strategy. We employed V-PADOX because it provides two SETs at the

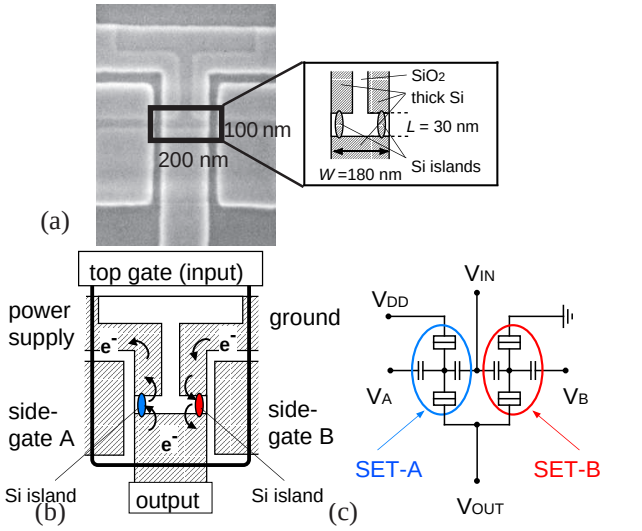


Fig. 12. Structure of the complementary single-electron inverter: SEM image (a) and its schematic views (b),(c). The top gate for the input covers the entire region shown in (a). In (b), the islands are indicated by the two ovals. The flow of electrons is indicated by the arrows. In (c), V_{IN} and V_{OUT} represent the input and output voltages. V_{DD}, V_A, and V_B are the voltages applied to the power-supply terminal and the two side gates, A and B.

same time, which simplifies construction of complementary logic circuits. (Actually, we used an improved version of V-PADOX, which gives us SETs connected in series instead of in parallel.) Figure 12 shows a SEM image (a), a schematic top view (b) and the equivalent circuit (c) of the complementary inverter. In Fig. 12(a), the bold rectangle encloses the key part of the circuit where the two SETs are formed. In Fig. 12(b), the top gate for the input, which is not shown in Fig. 12(a), is outlined by the bold line. Each SET has a side gate (A and B) to control the peak positions of its current oscillation. The two SETs are referred to as SET-A and SET-B. Figure 12(a) shows the input-output transfer characteristics of the inverter for a power-supply voltage V_{DD} of 20 mV. For this operation, we adjusted the side-gate voltages so that SET-A and SET-B work as p-type and n-type transistors, respectively. The voltage gain of the circuit is larger than unity as shown by the slope in Fig. 13(a). This larger-than-unity gain relies on the high-gain SETs formed by V-PADOX, and guarantees signal transfer to the following gates. Figure 13(b) shows the inverting operation for a square-wave input with an amplitude of 20 mV. The amplitude of the output is nearly the same as those of the input and the power supply voltage. Although the switching speed is low in this measurement, it is not limited by the inverter itself, but just by the slow response of the external circuit due to a large capacitance in the measurement system. If we put a smaller load capacitance, the inverter should operate faster as discussed in section **3.1**.

5.2. Single-electron transfer device

The ultimate low-power operation can be achieved if a single electron can represent a bit. Such kinds of single-electron logic circuits will consist of multiple-island struc-

tures. We tried to fabricate a SED with two islands by applying PADOX to a T-shaped wire structure on a thin SOI wafer (Fig. 14(a)) [20]. Each branch of the "T" was converted into a Si island because the branching point accumulates less stress and therefore becomes oxidized faster than the rest of the wire does. Two ultrafine gate electrodes were formed over the islands as shown in Fig. 14(b). Then a SiO_2 interlayer and an upper poly-Si gate that covers the entire region shown in Fig. 14(b) were successively formed. Figure 15 illustrates the schematic island structure and the simplified equivalent circuit of the device, where the island at the branch T_3 just acts as a lead because it is too large to operate as a Coulomb-blockade island at about 30 K. Therefore, this is a double-island device in which the two islands are capacitively coupled to each other. Figure 16 shows the current switching operation between I_1 and I_2, which occurs in response to a square-wave input upper-gate voltage V_{ug} with an amplitude of 100 mV. The current path is switched between the two branches because the Coulomb blockade against electron tunneling is set alternately at each island as the input upper-gate voltage changes between the high and low levels. In principle, this switching operation can be applied to a CMOS-type inverter or a double-through switch.

In this device, the two islands are capacitively coupled as indicated in the equivalent circuit shown in Fig. 15(b). By using the effect of this coupled capacitance, the so-called single-electron pump, which enables us to transfer electrons one by one, can be achieved [5, 20]. Moreover, fabrication of three capacitively-coupled islands in our T-shaped wire device gives us the directional switch for single-electron transfer shown in Fig. 17 [20, 21]. In this device, two single-electron pumps are merged so that a single electron is transferred via one of the two paths. This selection is determined

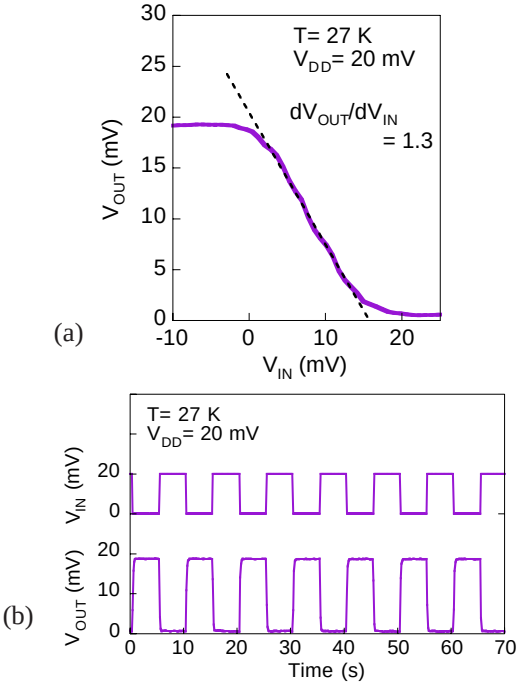


Fig. 13. Input-output transfer characteristics of the inverter (a), and the output voltage for a square-wave input voltage with an amplitude of 20 mV. The power-supply voltage is 20 mV for both (a) and (b).

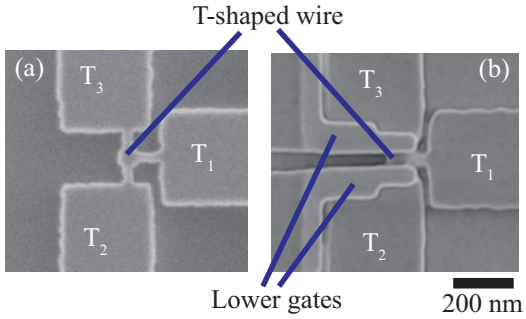


Fig. 14. SEM image of a T-shaped Si wire before PADOX (a) and the image after formation of two ultrafine gate electrodes on it (b). The width of the lower fine gate is 60 nm.

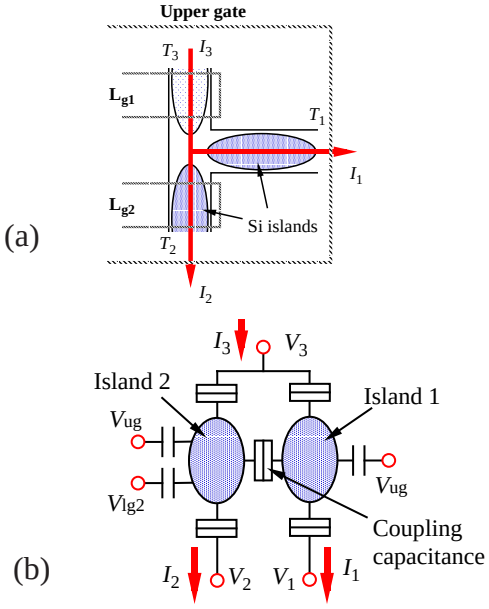


Fig. 15. Schematic structure of the T-shaped wire after PADOX (a) and the simplified equivalent circuit of the device (b). The biggest island, which is in branch T_3, just acts as a lead. The wide upper gate covers the wire region. The island in branch T_1 is controlled by the upper gate voltage (V_{ug}). The island in branch T_2 is controlled both by the lower gate voltage (V_{lg2}) and the upper one (V_{ug}).

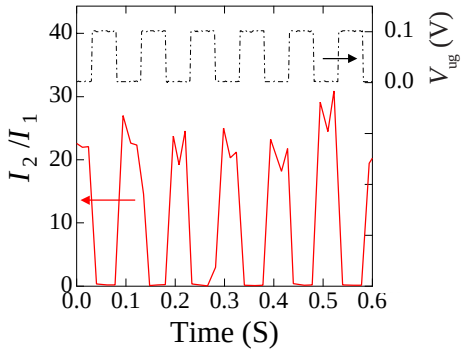


Fig. 16. Current vs. gate voltage characteristics of the T-shaped wire device measured at 33 K. The lower gate voltage V_{lg2} only affects the current I_2. Curves for different V_{lg2} are vertically offset for clarity.

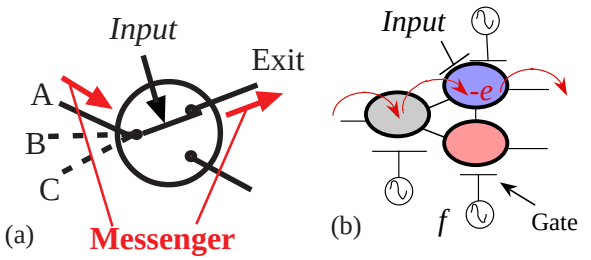


Fig. 17. Unit function of a directional switch for BDD circuit (a) and a schematic diagram of a single-electron-transfer device using three capacitively-coupled islands in a T-shaped wire (b).

by the input voltage signal V_{in}. This kind of operation can be applied to a binary decision diagram (BDD) circuit in which a single electron is used as a messenger.

5.3. Multigate single-electron transistor for multiple-valued logic

5.3.1. Exclusive-OR gate for binary logic

The SET has completely different characteristics from those of MOSFETs. One is that the SET can inherently have multiple gates while the usual MOSFET can not. Another feature is that the SET exhibits an oscillatory conductance as a function of the gate voltage. By exploiting these remarkable features, a new kind of functional device can be created. Figure 18 shows an equivalent circuit of a multigate SET in which several gate electrodes are connected to the SET island via gate capacitances. In this device with N input gates, the drain current $I_D(V_{in1}, V_{in2} \cdots V_{ini} \cdots Vin_N)$ is determined by the sum of $C_i V_{ini}$, as

$$I_D(V_{in1}, V_{in2} \cdots V_{ini} \cdots V_{inN}) = f(\sum_i^N C_i V_{ini}/e) , \quad (3)$$

where C_i is the capacitance between the SET island and the i-th gate electrode. The drain current takes a minimum when the sum $\Sigma C_i V_{ini}/e$ is an integer because the Coulomb blockade sets in. Here, $C_i V_{ini}/e$ corresponds to the number of excess electrons on the i-th gate electrode. Conversely, when the sum is a half integer ((2l-1)/2: where

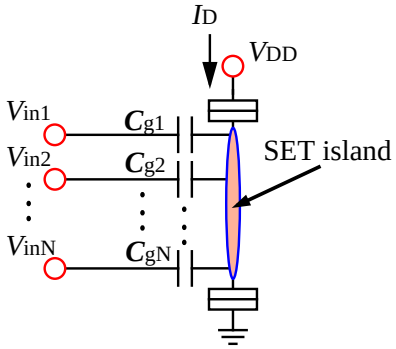


Fig. 18. Equivalent circuit of a multigate SET.

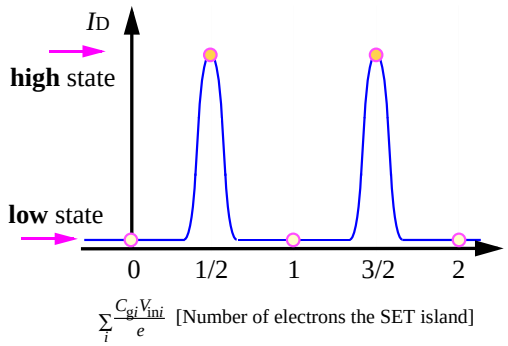


Fig. 19. Typical current vs. input gate voltage characteristics of a multigate SET. The horizontal axis is the sum of the products of each C_i and V_{ini}, which corresponds the number of excess electrons on the SET island.

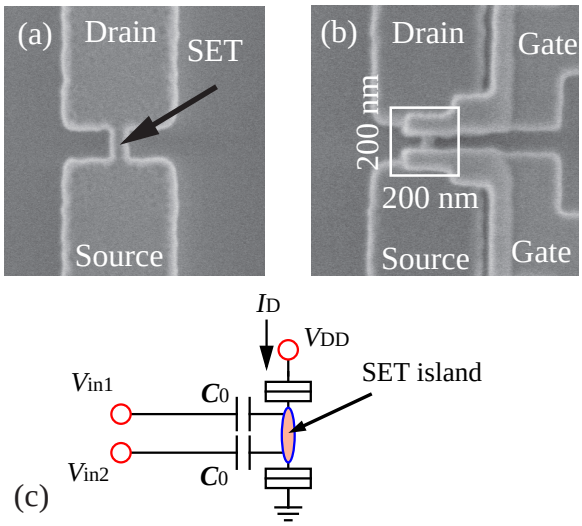


Fig. 20. SEM image of a Si wire before PADOX (a), the image after formation of two ultrafine lower gate electrodes (b), and its equivalent circuit (c). The wire length is 150 nm. The width of the fine gate is 60 nm. The active area of the XOR gate is within 200 x 200 nm^2.

l is an integer), the current flows because the Coulomb blockade is lifted. The function in eq. (3) indicates that the device can be used to construct a neural-circuit. In addition, we can realize another interesting operation by the use of oscillatory conductance characteristics.

Typical current characteristics of the multigate SET at a low source-drain voltage are determined by $\Sigma C_i V_{ini}/e$ as depicted in Fig. 19. For simplicity, we assume all the gate capacitances are the same C_0. Each gate voltage of $e/2C_0$ can switch the current level from high to low and vice versa. This means that an even number of "HIGH" gates creates the "LOW state", and an odd number the "HIGH state" when we use $e/2C_0$ as the "HIGH" input gate voltage level and 0 V as the "LOW" level. This is exactly the function of the Exclusive-OR (XOR) gate in the binary logic circuit [22, 23].

We fabricated such a device by using PADOX [23]. SEM

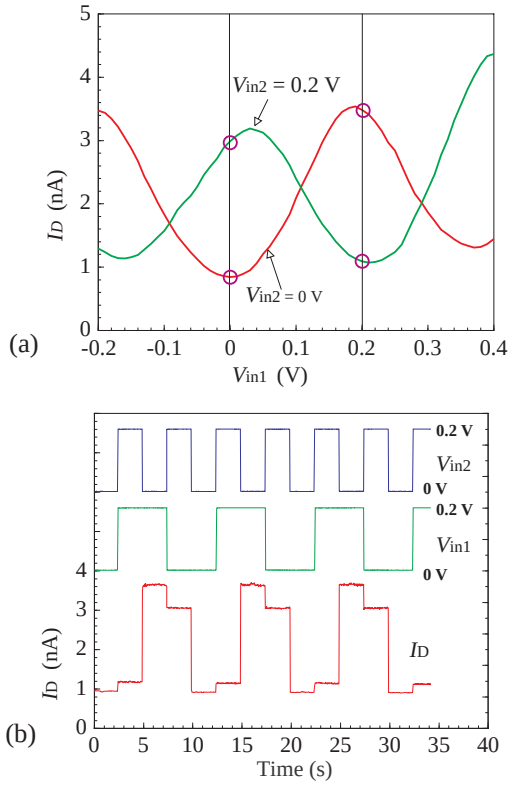


Fig. 21. Drain current of the dual-gate SET as a function of one of the lower gate voltages (V_{in1}) when the other lower gate voltage (V_{in2}) was 0 and 0.2 V (a) and the current switching characteristics of the SET when the input-gate voltages (V_{in1} and V_{in2}) were switched between 0 and 0.2 V (b). The measurements were made at 40 K and at a drain voltage of 10 mV.

images of the device are shown in Figs. 20(a) and (b). A small 1D Si wire fabricated on a SOI wafer (Fig. 20(a)) was converted into a small SET by means of PADOX. Then, using an electron-beam exposure system with a high overlay accuracy, two ultrafine poly-Si gate electrodes were attached so as to cover a part of this island as shown in Fig. 20(b). The equivalent circuit is shown in Fig. 20(c), where the two gate capacitances are almost equal due to the symmetric structure of the gates. The drain current oscillations of the device are shown in Fig. 21(a). The peak and valley positions of oscillation shift in the negative voltage direction when V_{in2} is 0.2 V. Figure 21(b) shows the drain current switching measured at 40 K in response to the switching of the two input-gate voltages between 0 and 0.2 V. Low current levels were obtained only when the input voltages were both high or both low. This represents an XOR-gate operation [23]. This function can be implemented with just one SET, whereas the XOR gate used in conventional CMOS logic circuits needs 16 transistors.

3-2. T-gate: multiple-valued multiplexer

The operation principle of the two-input XOR-gate for binary logic enables us to make a special pass transistor switch that becomes "on" only when the input signal takes on a particular value. The current output of the two-input XOR gate shown in Fig. 20(c) is written as

$$I_D(V_{in1}, V_{in2}) = f(C_0 (V_{in1} + V_{in2})/e), \qquad (4)$$

The SET is in its "on" state only when $V_{in1}+V_{in2}= (2l\text{-}1)e/2C_0$, where l is an integer, typically one. If one of the gate electrodes is used as the input gate and the other the control gate, the device transmits the current signal only at a particular input voltage. We can exploit the function to make a T-gate for multiple-valued logic. Figure 22 shows the proposed T-gate for radix-4 which can produce any output pattern depending on the input signals in radix-4. The circuit includes four two-input-gate SETs in which the voltages applied to the control gates are $2V_0$, V_0, 0V, and $-V_0$, respectively. Each SET turns on only when the sum of the input and control gate voltages is $e/2C_0$. Here, we assume the signal level as jV_0, where j is an integer of 0, 1, 2 or 3 and $V_0=e/4C_0$. The output current flowing through the SET as selected by V_{in} is determined by the applied drain voltage and load resistance R. Here, R must be larger than the resistance of the SET at the current peak and lower than the valley resistance of the SET. The output voltage V_{out} of the circuit can be determined as,

$$V_{out} = V_{i0} \quad \text{when } V_{in} = 0\,, \qquad (5)$$
$$V_{out} = V_{i1} \quad \text{when } V_{in} = V_0\,, \qquad (6)$$
$$V_{out} = V_{i2} \quad \text{when } V_{in} = 2V_0\,, \qquad (7)$$
$$V_{out} = V_{i3} \quad \text{when } V_{in} = 3V_0\,. \qquad (8)$$

Here, V_{i0}, V_{i1}, V_{i2} and V_{i3} should be lower than e/C_{total}. The relationship between the input voltage V_{in} and conductance of SET is shown in Fig. 23(a). Since there is no overlap in the "on" regions in the conductances, the channel of the current flow can be selected by V_{in}. For example, Fig. 23(b) shows the relation between V_{in} and the output current of the T-gate when V_{i0}, V_{i1}, V_{i2} and V_{i3} are 0V, $3V_{0I}$, $2V_{0I}$, and V_{0I}, respectively. Here, V_{0I} is a voltage lower than $e/4C_{total}$. As a result, by changing V_{in}, we can select the output current level that is the sum of the SET currents. This function indicates that the device operates as a four-valued T-gate that acts as a multiplexer to interleave or transmit four-valued

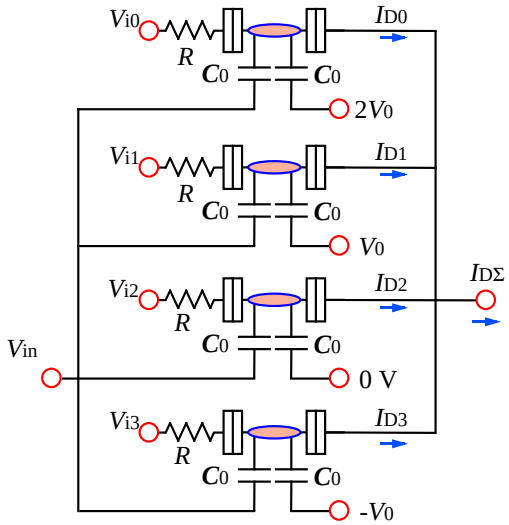


Fig. 22. Equivalent circuit of a T-gate for radix-4 that uses four dual-gate SETs.

current signals simultaneously to the output terminal according to the four-valued input signals.

The electrical characteristics shown in Fig. 21(a) are insufficient because the peak width is too wide to operate the T-gate for radix-4. To overcome this problem, we have to make the total capacitance of the SET island smaller than 1/2 that of the present one.

3-3. Ring sum for multiple-valued logic

The function of XOR for binary radix can be exploited to realize a ring sum circuit for multiple-valued logic. Figure 24 shows the equivalent circuit of an N-input ring sum for radix-3 logic. In this circuit, we set the control gate voltage of the upper and lower SETs to be $V_0/2$ and $-V_0/2$, respectively. The upper and lower circuits exhibit oscillatory currents as a function of the sum of the input gate voltages as shown in Fig. 25(a). Here, we have to set V_0 to $e/3C_0$. The upper SET becomes conductive when $\Sigma V_{\mathrm{in}i}/V_0 = (3n+1)$, where n is an integer. The lower one is conductive when $\Sigma V_{\mathrm{in}i}/V_0 = (3n+2)$. If we set the drain voltages of the two SETs to $V_{0\mathrm{I}}$ and $2V_{0\mathrm{I}}$, respectively, the output current becomes as shown in Fig. 25(b). The relation between the sum of the input voltages and the output current level is shown in Fig. 25(c). The output current I_{out} is written as

$$I_{\mathrm{out}} = a(V_{\mathrm{in}1}/V_0 \oplus V_{\mathrm{in}2}/V_0 \oplus \cdots \oplus V_{\mathrm{in}i}/V_0 \oplus \cdots \oplus V_{\mathrm{in}N}/V_0), \quad (9)$$

where a is a constant determined by drain voltage $V_{0\mathrm{I}}$ and load resistance R. This is actually the function of the ring sum of input voltages for radix-3.

The operation mechanism of the circuit can be expanded to those for radix-m. Figure 26 shows a circuit that realizes the function of an N-input ring sum for radix-m. Here, for the radix-m circuit,

$$V_0 = e/mC_0 , \quad (10)$$

and the voltages V_{C} for the control gate of i-th SET is set at

$$V_{\mathrm{C}} = (m/2\text{-}i)V_0. \quad (11)$$

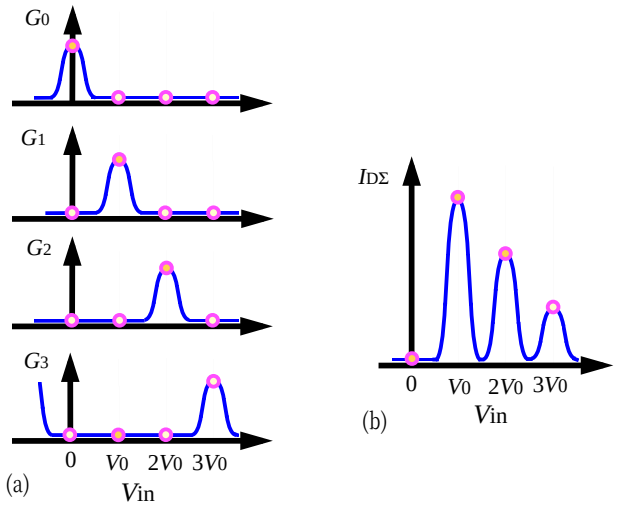


Fig. 23. Conductance characteristics of each SET (a) and the output current of T-gate (b) as a function of input gate voltage V_{in}.

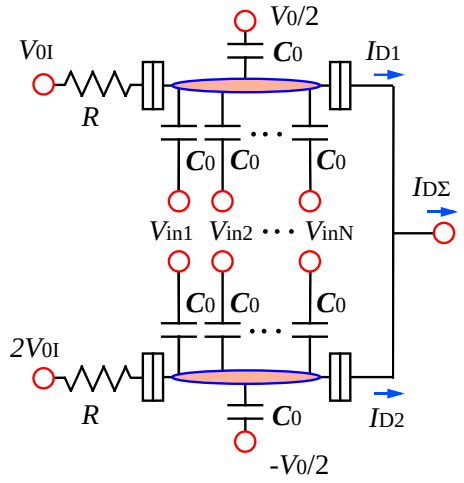
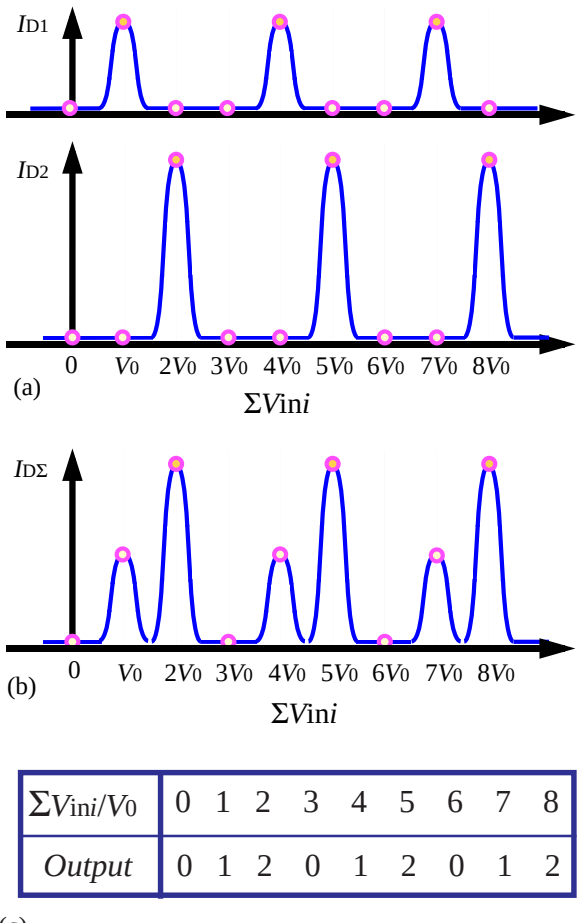


Fig. 24. Equivalent circuit of an N-input ring sum for radix-3 that uses two multigate SETs.



$\Sigma V_{\mathrm{in}i}/V_0$	0	1	2	3	4	5	6	7	8
Output	0	1	2	0	1	2	0	1	2

(c)

Fig. 25. Current characteristics of the two SETs of an N-input ring sum (a) and the output current of the adder as a function of the sum of the input gate voltages ($\Sigma V_{\mathrm{in}i}$).

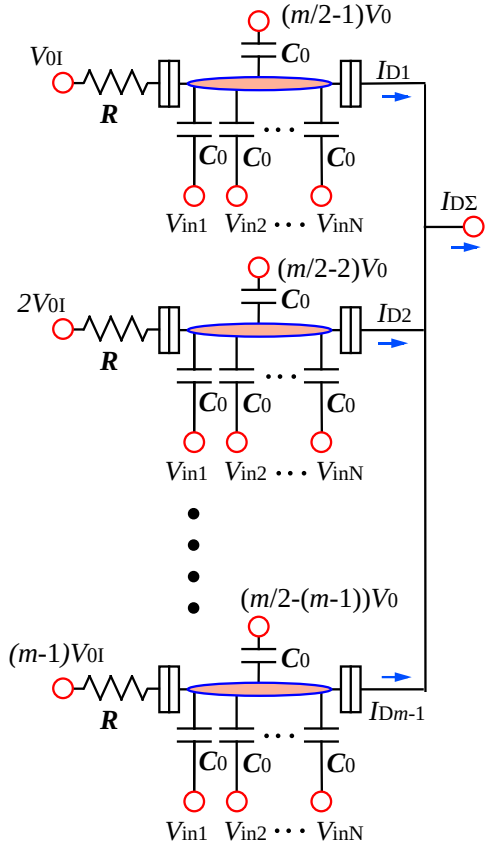


Fig. 26. Equivalent circuit of N-input ring sum for radix-m that uses m-1 multigate SETs.

It is remarkable that a very complicated function of the ring sum can be implemented by the use of only m-1 transistors. The function of a ring sum is useful to constructing a residue number system for multiple-valued logic.

6. Conclusion

We developed two special methods of fabricating Si SEDs. The PADOX and V-PADOX methods utilize a special oxidation phenomenon that occurs when a very small Si structure is thermally oxidized. This phenomenon enables us to fabricate small SEDs in a self-aligned manner. We fabricated several memory and logic devices. The results demonstrate that PADOX and V-PADOX have great flexibility when it comes to fabricating various types of single-electron devices and should be very useful in the development of single-electron LSIs. In this paper, we proposed new ways of applying multigate SETs to multiple-valued logic circuits, such as the T-gate and ring sum.

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