EE510H Assignemnt 1: 8 entry 8 bit unsigned integer sorter

Ram Koganti Khader Mohammad
{rkoganti,kmohamm}@ichips.intel.com

1 Logic Description

This sorter circuit sorts 8-bit unsigned integers. The sorter circuit remembers the last eight entries input into the sorter. The designed entity is shown in the figure 1.

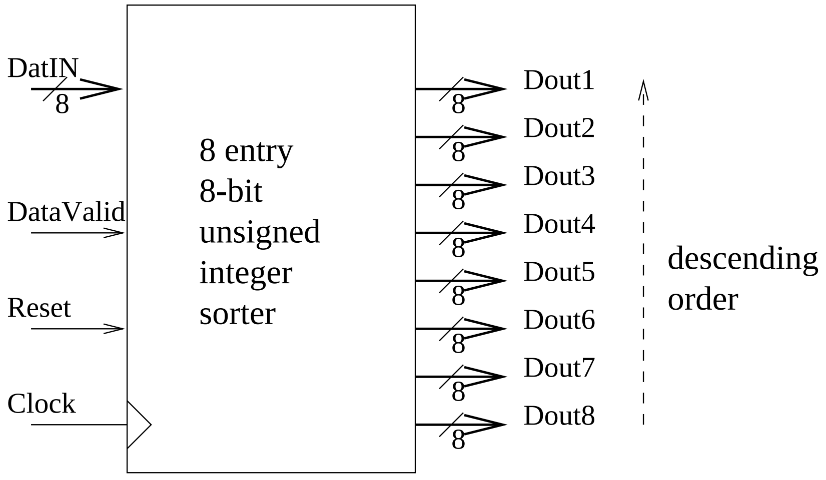

Figure 1: Eight entry 8-bit unsigned integer sorter

The circuit consists of eight 8-bit registers, with enable and reset pins. The control circuit uses the insertion sort algorithm. A description of the algorithm is shown in figure 2.

There are basically three operations done on the registers.

- Shift in Previous Registers Data

- Recycle Register Value
- Load Input Data

If the Register value is larger than the input data than the data in the register is recycled. The only exception is the last register, which is never recycled.
If the Register value is smaller or equal to the input data and the previous Registers value is lesser or equal too, then the data is shifted in, from the previous register.
If the Register value is smaller than the input data but the previous Registers value is greater than, the input data is loaded into the register.

A mux is used to load the correct data into the register. The Mux Select Signals are generated by the control logic, that basically consists of a "greater-than" comparator.

The above operations are encoded into two bits with the following opcode assignment: Shift (00), Recycle (11) and Load (10).

The circuit uses the concept of a generalized register. The control logic is an iterative network. The complete implementation of a 4 entry sorter is shown in figure 3.

2 VHDL

We applied top down design methodology to this logic circuit. Fisrt we coded the basic entities, the "greater-than" comparator, the 8-bit register with a synchronous enable and an asynchronous reset, and the Multiplexor.

Next we designed a generalized sorting register that consisted of the 8-bit register, mux, comparator and an OR gate.

Finally, we instantiated the generalized sorting register eight times to create the 8-entry sorter.

NOTE: All the sub-circuits were simulated using NOVA, but the 8 entry sorter was not simulated because it could not be fit into the largest available CPLD device and NOVA can do only post-fitted device timing simulation.

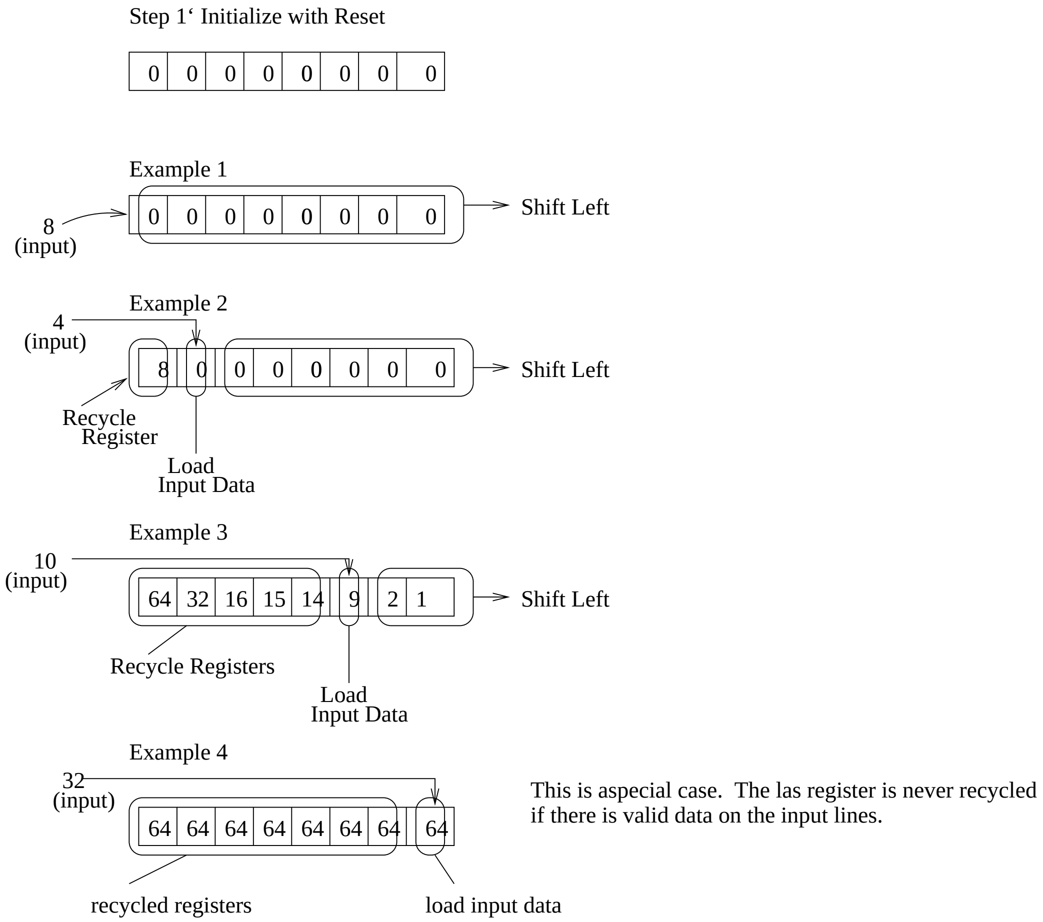

Figure 2: Sorting Algorithm Description