

#### Prof. K. J. Hintz

#### Department of Electrical and Computer Engineering George Mason University

1



#### Arrays

- Single and multi-dimensional
- Single Type
- Records– Mixed types



- Indexed Collection of Elements All of the Same Type
  - One-dimensional with one index
  - Multi-dimensional with several indices



#### Constrained

- » the bounds for an index are established when the type is defined
- Unconstrained
  - » the bounds are established after the type is defined
- Each position in the array has a scalar index value associated with it

### Array Definition Syntax

array ( discrete\_range { , ... } )
of element\_subtype\_indication ;

#### *discrete\_range* is an index

 name of previously declared type with optional range constraint

### Array Declaration, *e.g.*,

type Large\_Word is array ( 63 downto 0 )
 of bit ;

type Address\_List is array ( 0 to 7 ) of Large\_Word ;

### Array Declaration, e.g., type 2D\_FFT is array ( 1 to 128, 1 to 128 ) of real ; type Scanner is array ( byte range 0 to 63 ) of integer ;

type Sensor\_Status is array
 ( Stdby, On, Off ) of time ;

**Unconstrained Declaration** type Detector\_Array is array natural range <> ) of natural ; ■ The symbol '<>' is called a box and can be thought of as a place-holder for the index range.

Box is filled in later when the type is used.
variable X\_Ray\_Detector : Detector\_Array
 ( 1 to 64 );

## Predefined Unconstrained Types

### type string is array ( positive range <> ) of character ;

#### type bit\_vector is array

( natural range <> ) of bit ;

### Predefined Unconstrained Types

type std\_ulogic\_vector is array
 ( natural range <> ) of std\_ulogic ;

### type bit\_vector is array ( natural range <> ) of bit ;

### Unconstrained Array Ports

#### ■ 1. Specify Port As Unconstrained

### 2. Index Bounds of Signal Determine Size of Port

#### *e.g.*, AND Gates With Different Number of Inputs

## 1. Unconstrained Array Port, *e.g.*,

#### entity And\_Multiple is

port ( i : in bit\_vector ;
 y : out bit );

#### end entity And\_Multiple ;





```
architecture And_Multiple_B of
 And_Multiple is
begin
 And_Reducer : process ( i ) is
  variable Result : bit ;
  begin
   Result := '1';
   for Index in i'Range loop
  _{\star} Result := Result and i ( Index ) ;
   end loop ;
```

variable

Copyright © 1997/8/9, KJH, 545\_5, 5/7/2001

Signal created outside the loop



# y <= Result ; end process And\_Reducer ; end architecture And\_Multiple\_B ; signal</pre>





#### The Input Port Is <u>Constrained</u> by the Index Range of the Input Signal, *i.e.*, An 8-Input AND Gate.

### Array References

- Arrays <u>Can Be Equated</u>, Rather Than Having to Transfer Element by Element
- Refer to Individual Elements By
  - Single Index Value, *e.g.*, A ( 5 )
  - Range: a contiguous sequence of a onedimensional array can be referred to by using it as an index. *e.g.*, A( 5 to 15 )
  - Previously defined subtype
  - Index types do not have to be the same

### Array Aggregate Syntax

#### A List of Element Values Enclosed in Parentheses

#### Used to Initialize Elements of an Array to Literal Values

aggregate <= ( [ choices => ] expression { ... } )

### Array Aggregate

- Two Ways of Referring to Elements
  - Positional: explicitly list values in order
  - Named Association: Explicitly list values by their index using "choices"
    - » Order NOT important
- Positional and Named Association Cannot Be Mixed Within an Aggregate.

type Sensor\_Status is
array ( Stdby , On , Off ) of time ;

#### variable FLIR\_Status :

Sensor\_Status := ( 0 sec , 0 sec , 0 sec );

variable FLIR\_Status :
 Sensor\_Status := ( On => 5 sec ) ;

- others Can Be Used in Place of an Index in a Named Association,
  - Indicating a Value to Be Used for All Elements
     Not Explicitly Mentioned

variable FLIR\_Status : Sensor\_Status :=
 ( Off => 10 min, others => 0 sec ) ;

A Set of Values Can Be Set to a Single Value by Forming a List of Elements Separated by Vertical Bars, |.

type 2D\_FFT is array
 ( 1 to 128, 1 to 128 ) of real ;
variable X\_Ray\_FFT : 2D\_FFT :=
 ( ( 60, 68 ) | ( 62, 67 ) | ( 67, 73 )
 | ( 60, 60 ) => 1.0 , others 0.0 ) ;

One-Dimensional Arrays of Bit or Boolean

Element by element AND, OR, NAND, NOR, XOR, XNOR can be done on array

**Array Operations** 



### Array Operations, *e.g.*,

Samp\_2 := Samp\_1 and Bit\_Mask ;

Bits from 8 to 15 are AND-ed with Bit\_Mask

# Complement of elements of a single array, NOT

**Array Operations** 

Samp\_2 := not Samp\_1 ;

#### One-Dimensional Arrays Can Be Shifted and Rotated

- Shift
  - » Logical: Shifts and fills with zeros
  - » Arithmetic: Shifts and fills with copies from the end being vacated

**Array Operations** 

– Rotate

» Shifts bits out and back in at other end



### One-Dimensional Arrays Can Be Operated on by Relational Operators,

**Array Operations** 

= , /= , < , <= , > , >=

- Arrays need not be of the same length

– Arrays must be of same type

### **Array Operations** Concatenation Operator, & – Can combine array and scalar B" 1010\_1100 " & B" 1100\_0000 " == B" 1010\_1100\_1100\_0000 " B" 1010\_1100 " & `1' == B" 1010\_1100\_1 "

### Array Type Conversions

- One Array Type Can Be Converted to Another If:
  - Same element type
  - Same number of dimensions
  - Same index types

# Array Type Conversions, *e.g.*,

Example

subtype name is string ( 1 to 20 ) ;
type display\_string is array ( integer
 range 0 to 19 ) of character ;
variable item\_name : name ;
variable display : display\_string ;
display := display\_string ( item\_name ) ;

Assignments Can Be Made From a Vector to an Aggregate of Scalars or Vice-Versa.

type Sensor\_Status is array
 ( Stdby, On, Off ) of time ;

variable Stdby\_Time, On\_Time, Off\_Time :
 time ;



( Stdby\_Time, On\_Time, Off\_Time ) := Flir\_Status ;

# Records

#### Collections of Named Elements of Possibly Different Types.

#### To Refer to a Field of a Record Object, Use a Selected Name.



#### Aggregates Can Be Used to Write Literal Values for Records.

#### Positional and Named Association Can Be Used

 Record field names being used in place of array index names.

#### type instruction is record op\_code : processor\_op ; address\_mode : mode ; operand1, operand2 : integer range 0 to 15 ; end record ;

Record *e.g.*,\*

#### \*Ashenden, VHDL cookbook

# End of Lecture

