- CLASS
- GRADING
- HOMEWORKS
- PROJECTS
- REVIEW OF DIGITAL LOGIC

Digital Design using VHDL and Verilog

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Introduction

- Administration
- About Review
- RASSP Program
- Why VHDL?
- Flip-Flops (see ECE 271 class slides)
- Shift Registers
- Generalized Register
- Pipelined Sorter

Administration

- Instructor: Prof. Marek A. Perkowski

- Course Information
  - My home page `http://ee.pdx.edu/~mperkows`
  - Computer Engineering web site
    - `http://ede.pdx.edu`

Administrative

- Office
  - Portland Center for Advanced Technology, Room 146
- Office Hours
  - Mondays 12-1pm
  - Fridays 6 pm - 9 pm - meetings in CECS Annex or as announced to be streamed
  - Other Times by Appointment
- Office Phone
  - (503)725-5411 (Answering Machine)

Administrative

- Email
  - mperkows@ee.pdx.edu
- Students with Disabilities
  - If you need special assistance, please inform me soon so that we can work something out.
- There is a milestone chart available on the class web site.

Grading

- HW 35%
  - Assignments are on the web
- Final Project 65%

Grading

- Attendance at Lecture
  - Not graded
- Makeup Exams
  - Makeup exams are not given.
  - Project should be completed before end of the class because I will leave Portland for 1.5 years

Homeworks

- Homeworks Require Use of VHDL

- Mentor Graphics Tools
  - contact support (cat) people
  - use any lab
  - use addpkg

Resources

- IEEE Interactive VHDL Tutorial
  - On-line on Computer Engineering Home page
  - http://cpe.gmu.edu
  - password protected
- IEEE Standard 1076-1993
  - find using search engines on WWW
- Use my WWW Page resources, too much to digest.

Resources

- Cypress Semiconductor (Warp release 5.x)
  - PC-based
  - $99 with textbook
  - Oriented towards Their PLD & FPGA devices
  - VHDL Subset simulator
- Xilinx FPGA
  - Student edition
  - Schematic, FSM, VHDL

Honor Code

- You Are Encouraged to Collaborate With Other Students in Projects.
- Final VHDL code for each Homework should be done by yourself.
- Exams Are Closed Book, Closed Notes, and the Normal Honor Code Applies to All Exams.
- No exams this year.

Required and Additional Textbooks

- *Required and recommended*
  - *see my web page*
- *Additional*
  - *The Designer's Guide to VHDL*
    - Peter J. Ashenden
    - Morgan-Kaufman
    - ISBN 1-55860-270-4 (paperback)
    - LOC TK7888.3.A863
    - Dewey Decimal 621.39'2--dc20
    - 1996

Projects for year 2002

- **1. Speech Recognition for a robot (new)**
- **2. Reversible Cube Calculus Machine (continuation)**
- **3. Combined DSP and Cube Calculus Machine (continuation)**
- **4. Decomposition Machine (continuation)**
- **5. Satisfiability Machine (continuation)**
- **6. Rough Set Machine (continuation - Torrey Lewis)**
- **7. Convolutional Image Processor (continuation)**
- **8. Sorter/Absorber (continuation - Kashubin)**
- **9. Controller of a Robot (new)**
- **10. Evolvable Hardware (new)**

These are just examples, more projects will be added, you can propose your own project.