- Mentor Tools tutorial
- Bold Browser
- Design Manager
- Design Architect
- Library Components
- Quicksim
- Creating and Compiling the VHDL Model.

Introduction To Mentor Graphics

- Mentor Graphics BOLD browser allows to access manuals.
- Design Architect is used for schematic capture.
- QuicksimII is used for simulating digital logic and microcomputer circuits.
- To add the package type: ‘addpkg’ at the prompt.
  - Note the number to the left of the Mentor tools, and enter it.

Connecting To Mentor Tools at PSU

- For the first time to add package to your account : Type ‘addpkg’ command at the Unix prompt.
- When the list appears find Mentor and note the number besides it.
- Enter the number and press return key.

Invoking The Design Manager

- Design Manager allows to access all the available tools from one integrated environment.
- After logging in, type the following :
- ‘ setenv MGC_WC/u/your_user_name’ at the prompt and press return.
- After this type ‘dmgr’ which will invoke Design Manager.

Invoking Design Architect

- After you invoke Design Manager:
  - the central portion of the window shows the entry for each file in your home directory,
  - the left side shows icon for the Mentor Graphics tools.
- Using scroll bar find icon for **Design Architect** and left click it.

Opening A Sheet And Setting Grid Spacing

- To open a Sheet click on Open Sheet icon from Session_palette of the Design Architect, which appears at the right corner.
- Enter the **component name** which corresponds to the filename in the open sheet form.
- A window will appear with grid of dots and plus signs.
  - The default setting is 0.25 inches mark off the dots and plus sign.

Opening The Sheet And Setting Grid Spacing.

- With the default setting the plus sign mark off and dots mark off are 0.25 inches.
- You can change the setting by putting the cursor on Setup entry along the Design Architect window and clicking on page entry, and writing the new setting in the page form's Pin Space box.
- To change the grid spacing click on Grid entry of Setup entry and repeat the procedure.

Opening The Sheet And Setting The Grid Spacing

- Click on Open Sheet icon from Session_palette section of **Architect window** which appears a the right hand corner.
- On the open sheet form, type the name of the component, and click O.K.
- After which a window appears which has dots and plus sign.

Adding A Border And Title

- To add a Rectangular border ➡ Edit entry Edit Command ➡Add command ➡Rectangular Box.
- Repeat the same procedure to add the Title box.
- To have a center line of the title box ➡ Edit Edit Command ➡ Add Command ➡ Line.
- To put some text in the title block ➡ Edit Edit Command ➡ Add Command ➡ Text.

Adding Text

- To add some text in the title box: ➡ Edit Edit Commands ➡ Add Comment ➡ Text Command.
- The default height for the text is small,to change it: ➡ Edit ➡ Edit Command Change Attributes ➡ Text ➡ Height Command

Getting And Placing The Library Component

- Drawing the schematic, we use the component from two libraries which are accessed through the Libraries entry at the top of the Design Architect window.
- For Logic devices we use the models from Logic Modeling Corporation.
- For Vcc, ground, portin and portout connectors we use Mentor Graphics **misc_lib.**

Library Component

- Logic Modeling Corporation Components : Libraries entry ➡ LMC SmartModels
- Clicking will list major LMC component sublibraries, in the right side of the window.
  - Choose the appropriate logic entry.
- To go back to the previous menu from the current one of the logic entry, put the cursor in a blank section of the window containing the list, with the help of right key pop up the palette & go back.

Library Component

- Palette menu doesn’t have a default scroll bar.
- To add one, pop up the Palette menu and choose Show Scroll bars.
- Gates are chosen from the library according to the need. Portin, portouts,Vcc components are added from Mentor misc Library.
  - To get this library: Libraries Menu ➡ MGC_Digital Library
- The list will appear at the right hand corner. Choose misc_lib entry.

Drawing Nets (Wires)

- To draw wires : Add Menu ➞ Wire.
- When the menu disappears the cursor changes to ✤
- Move the cursor where to connect the wires.
- Press Esc key/cancel when done otherwise you will be in the net drawing mode.
- To exit from the net editor press the cancel button at the bottom of the schematic window.
- To make a back up of the sheet,use File ➞ Save

Checking And Quitting The Sheet

- Before plotting the schematic check the sheet by Sheet ➡ With Default.
- If report shows no errors ,close the report.If it shows some then correct them.
- Save your sheet and then for quitting the Design Architect Menu ➡ Quit.
- This will close the Design Architect window but “orphan” command will be left,to close it,move the cursor into the window,hold Control key & press C.use same for Design Manager.

Setting Up The Design Viewpoint

- Mentor Graphics define the Design Viewpoint as a set of rules used to establish the configuration of your design.
- Steps to create the proper design viewpoint reference for the QuickSimII simulator & the Logic Modeling Corp. models.
- Design Manager ➡ Design Viewpoint Editor (DVE) ➡ Double click
- When window appear ➡ OPEN VPT on right & click.

Starting QuickSim And Setting Up window

- For starting : Design Manager Tools ➡ QuickSim
- In the top box of the window type filename. Timing Mode Delay ➡ Detail of Delay ➡ Visible
- Read the contents of the small Model Message window after QuickSim window appears.
  - it should just contain a short message identifying Logic Modeling Corporation.
- Choose QuickSim from blank region of the window and then open ➡ sheet

Starting QuickSim

- Add a window which displays logic analyzer type traces of your stimulus signals and the resulting output signal(S)
- To start QuickSim ➡ Add ➡ Traces ➡ choose specified.
- Add traces form appears .
  - click on Named signals and then write names.
- In Trace window note that the signal names along the left side and time scale along the bottom .
  - Very similar to the timing display of a logic analyzer.

Starting QuickSim

- Helpful to have the input and output signals displayed in a list format as well as in the waveform format.
- To produce list: ➡ QuickSim
  Add ➡ List menu ➡ choose specified.
- When form appear click ➡Named signals ➡Fill the signal names.

Creating Input Stimulus Signals For Verifying The Logic

- To thoroughly test the logic of the circuit you need to apply each of the possible combinations to the inputs and check if the output is correct.
- The most common way to generate input stimulus signals in QuickSim is with Forced commands.
  - you can force a single value on a signal line or force sequence of values(multiple) on a signal line or force a repetitive signal called a “clock” on a signal line.

Running A Simulation And Viewing The Results

- To run the simulation pop up ➡ QuickSim Run ➡ Simulation Menu ➡ Choose Until Time.
- Write a time in the Until Time box form for one complete input waveform.
- Input and Output waveforms should appear in the trace window and a truth table type display should appear in the list window.
- To Change the view & the scale of the trace. Popup QuickSim ➡ View menu ➡ Zoom out/in.

Running the Simulation

- Study the the waveform to determine the glitch and scroll the display so that you can see the input signal transition which causes the glitch.
- Activate the list window which shows an entry for each time where an input or output signal changes.
- Use the list entry to find the maximum propagation delay for the circuit.

Adding Probes To Circuit And Running The Simulation.

- To see the trace of the signal on a particular line when run the simulation from 0 time, we can add probe to the output of the gate.For this choose QuickSim ➡ Add menu ➡ Probe.
- To add a trace for the probe: QuickSim ➡ Add menu ➡ Trace ➡ Choose Specified.
- To delete the trace: QuickSim ➡ Delete.

Creating And Compiling The VHDL Model

- We use Mentor Tools to create schematics for circuit designs containing parts from the Logic Modeling Inc. libraries and simulate those designs.
- For the cases where a commercial model is not available for a particular device, we can use VHDL.
- The VHDL model can be simulated directly or included in a design containing commercial models and simulated along with these.

Creating And Compiling The VHDL Model

- To start with the VHDL here are the steps:
  - Set the environment variables and bring up dmgr.
  - Invoke Design Architect.
  - Type the VHDL code.
  - After you finished with the code, compile it with compile option from the menu.
  - While compiling if the error comes,locate the errors ,by putting the cursor on the error message in the compiler window and click to select .

Generating A Schematic Symbol For A VHDL Model

- Open the Design Architect session palette and choose OPEN SYMBOL.
- In the form type ‘andor’ as the component Name.
  - Symbol which represents your VHDL design will appear in the Symbol Editor window.
- Pop up : Setup ➡ Grid ➡ Report ➡ Color ➡ Choose Grid.
  - Enter 1 in the Grids per Pin box & 10 in the Major Multiple box.
- To get some space around the symbol zoom out.

Generating A Schematic Symbol

- To give the name to the symbol: ➡ Add menu Properties.
- When form appears type MODEL in the new property Name box,and ‘andor’ in the Property Value box.
- Pop up : check menu ➡ defaults.
- Pop up : File menu ➡Save ➡ Default registration.
  - Again check,and close the symbol editor window.