

Design of Low Power CMOS Circuits with Energy Recovery

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Abstract

In view of changing the type of energy conversion in CMOS circuits, this paper investigates low power CMOS circuit design which adopts gradually changing power clock. First, we discuss the algebraic expressions and the corresponding properties of clocked power signals, then a clocked CMOS gate structure is presented. The PSPICE simulations demonstrate the low power characteristic of clocked CMOS circuits using trapezoidal power-clock. Finally, this paper also explores the design of sequential circuit, which adopts flip-flop with clocked power.

I. Introduction

The power dissipation in CMOS circuits is related to the type of energy conversion. In static CMOS circuits, a DC power supply is used and switching signal values is realized by charging and discharging the node capacitance. During this process, the charge is drawn from the power supply V_{dd} , then transported to node capacitance, and returned to the ground terminal, resulting in an irreversible energy conversion from electric energy to heat. As a result, when a node capacitance is charged (or discharged), it leads to an energy dissipation of $\frac{1}{2}CV_{dd}^2$ occurs.^[1] So reducing the energy dissipation has been equated to reducing the switching activity. Low power design targeting minimum switching activity has made significant progress in recent years.^[2] However, the obtained energy saving is still limited.

An energy conversion is needed to represent a change in signal value. If energy exists only in one form, i.e., electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e., magnetic field energy, into the digital circuit. If we relate the signal change to the conversion of electric energy to magnetic energy the so-called “energy-recovery” can be realized, by which the irreversible conversion from electric energy to heat caused by dissipative elements, i.e., resistors is largely reduced or avoided.

The energy conversion from electric field to

magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be alternating quantities. The latter has been extensively used in dynamic CMOS logic, clocked CMOS logic, and various domino logics.^[1] However, those circuits still rely on DC power, and the energy conversion remains as electric energy to heat. Therefore, we should further study the case of circuits supplied with AC power. The AC power controls the working rhythm of the circuit and acts as the clock, so we will call it the power-clock. The research shows that if the adopted power clock with gradually changing process during its rising and falling, only less energy is dissipated for charging and discharging the node capacitance through the conducting MOS transistor. Therefore, the called “adiabatic” switching operation is resulted, by which a new approach to design low power CMOS circuits is proposed.

Clocked CMOS circuits with gradually rising and falling power-clock are expected to obtain a significant energy saving. It attracts many researchers to study this issue in recent years^[3-11]. However, the operational constraint that the output signal should track the power-clock’s gradually rising and falling behavior to accomplish the charging and discharging process increases difficulty in the circuit design. At present, the existing research either adopts retractile cascade power clock or adopts multiple-phase power clock with memory schemes. Obviously, their applicability is awfully limited. We think that a new research on the energy recovery CMOS circuit should start from its basic theory, including the basic algebraic expressions and the basic properties of clocked signals. At the same time, both the basic clocked CMOS gate and the clocked flip-flop, the basic unit of energy-recovery CMOS circuits, should be investigated at the beginning. With the above view this paper will focus on these two topics.

II. An algebra for clocked signals

For simplicity, we assume that the clock is a symmetric square-wave. When $clk = 1$, the clocked signal displays its true logic value; when $clk = 0$, the clocked signal is forced to its “base” value, 0 or 1. For the

pre-charge circuits, the base value is 1 whereas for the pre-discharge circuits, the base value is 0. Therefore, in every clock cycle, the clocked signal is divided into two stages: set base (B) when $clk = 0$ and evaluate (E) when $clk = 1$.

Figure 1 shows a pair of complementary signals x/\bar{x} and the corresponding clocked signals. The values of x/\bar{x} in Fig.1 are (101101)/(010010); they could be regarded as the synchronous outputs of a falling-edge triggered-flip-flop. x/\bar{x} are however not clocked signals. In Fig.2, $x^{·clk}$, $\bar{x}^{·clk}$, x^{+clk} and \bar{x}^{+clk} are four clocked signals derived from x/\bar{x} . Notice that the superscript i in the exponent expression of x^i , $i \in \{·clk, +clk\}$, represents the logic relation between the original signals x/\bar{x} and the clocks clk/\overline{clk} . That is, $x^{·clk}$ is $x \cdot clk$, x^{+clk} is $x + \overline{clk}$, and so on. Obviously, the function of ($\cdot clk$) and ($+clk$) is to set the clocked signal during the B stage to base “0” or base “1”, respectively.

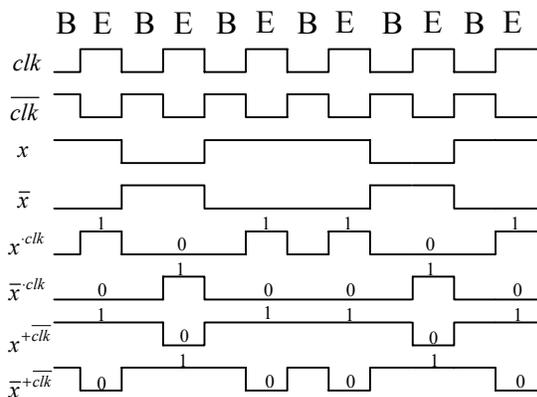


Figure 1. Clock and clocked signal

The following inverting relationships between the four clocked signals can be observed (cf. Fig.1):

1. Logic value inverse (with the same base), such as $x^{·clk}$ and $\bar{x}^{·clk}$; x^{+clk} and \bar{x}^{+clk} .
2. Base inverse (with the same logic value), such as $x^{·clk}$ and x^{+clk} ; $\bar{x}^{·clk}$ and \bar{x}^{+clk} .
3. Complete inverse, such as $x^{·clk}$ and \bar{x}^{+clk} ; $\bar{x}^{·clk}$ and x^{+clk} .

Figure 1 also shows that:

$$\bar{x}^{·clk} = \bar{x}^{+clk}, \quad \overline{\bar{x}^{·clk}} = x^{+clk}. \quad (1)$$

In line with the above-mentioned exponent expressions, the power supply V_{dd} (1), the ground (0) and the clock (clk/\overline{clk}) satisfy the following clocked expressions:

$$1 = 1^{+clk}, \quad 0 = 0^{·clk}, \quad (2)$$

$$clk = 1^{·clk}, \quad \overline{clk} = 0^{+clk}. \quad (3)$$

If we regard the exponent operation as a Boolean operation, then Eq.(2) and Eq.(3) can be easily proved. Furthermore, we can also prove the following expressions:

$$\begin{cases} (x \cdot y)^{·clk} = x^{·clk} \cdot y^{·clk} \\ (x \cdot y)^{+clk} = x^{+clk} \cdot y^{+clk} \end{cases}, \quad (4)$$

$$\begin{cases} (x + y)^{·clk} = x^{·clk} + y^{·clk} \\ (x + y)^{+clk} = x^{+clk} + y^{+clk} \end{cases}. \quad (5)$$

The physical meaning of the above Eq.(1) - Eq.(5) can be explained as follows:

1. Eq.(1) represents the De Morgan's Law. It shows that the inverter function applied to clocked signals produce the complete inverse of the original clocked signals (i.e. both the logic value and the base are inverse).
2. Eq.(2) shows V_{dd} (1) and ground (0) can continually work in the clocked circuits of base 1 and base 0, respectively.
3. Eq.(3) indicates that clk can assume the role of power supply in the clocked circuit of base 0, whereas \overline{clk} can assume the role of ground in the clocked circuit of base 1.
4. Eq.(4) and Eq.(5) suggest that the clocked signals which participate in the AND/OR operations, should have the same base, and the result is equal to the original signals being ANDed/Ored together, then clocked by the same base. Furthermore the result of NAND and NOR operations inverts the base according Eq.(1).

III. Clocked CMOS gate circuits

From the discussions in the previous section, we see that the clocked signals can be obtained by ANDing/ORing the original signal x with clk/\overline{clk} . However, there is no original signal x in our research circuit, which adopts gradually changing power clock. The input and output signals in the circuit are all clocked signals.

Thinking that the basic circuits in clocked CMOS circuits are also the gates, we first investigate the structure of clocked gates and their working principle. Similar to the traditional CMOS gates the outputs of the clocked CMOS gates should be “restored”, too. For traditional CMOS gates, the outputs are always clamped to either the power supply by conductive pMOS transistor for the high-

level output or the ground by conductive nMOS transistor for the low-level output, whereby the level-restoration is realized. Correspondingly, the outputs of the clocked CMOS gates should also be “clamped” to the power clock by conductive MOS switch to obtain “pulse”-restored outputs. Because of the alternating characteristic of power clock, this MOS switch should be the complementary CMOS transmission gate.

From the relationships among four clocked signals shown in Fig.1, we can find that a pair of complete inverse clocked signals $x^{clk} \square \bar{x}^{+clk}$ can be used to control the pMOS and nMOS of the transmission gate respectively, and then the another pair of complete inverse clocked signals $\bar{x}^{clk} \square x^{+clk}$ can be generated when clk and \overline{clk} are transmitted. On the other hand, the latter pair of clocked signals can be used to control the transmission of clk and \overline{clk} to reproduce the former pair of clocked signals. From the above analysis, we can derive the circuit shown in Fig.2(a). The relationships between the input and output in the circuit can be summed up as follows:

1. A pair of clocked signals to control a transmission gate should be physically complementary. Among them, the base-0 and the base-1 signal control the pMOS transistor and nMOS transistor respectively;
2. The output generated from clk is the base-0 signal, and is logic inverse to the input base-0 signal acting on the pMOS transistor. On the other hand, the output obtained from \overline{clk} , is a base-1 signal, and is logic inverse to the input base-1 signal acting on the nMOS transistor;
3. For any four unrestored clocked signal forms of a signal, its four restored clocked signals can be obtained by using two transmission gates to transmit power clocks clk and \overline{clk} .

By using trapezoidal power-clock, we PSPICE-simulated the circuit in Fig.2(a) with 2μ CMOS technology. The result is given in Fig.6(b) where we find that the output node signals do not maintain a even high top or even low bottom when the transmission gate shuts down. Take x^{+clk} as an example for explaining, clk does not immediately jump to high-level when x^{+clk} is dropping. The nMOS transistor in the transmission gate is still turn-on at that moment, so the output tracks clk and rises until the nMOS transistor shuts down completely. However, the simulation has verified that these uneven outputs does not affect the next stage. Figure 2(c) shows the energy dissipation curve of one-stage circuit in the use of the trapezoidal power-clock with clocked input sequence pair (01010) and (10101). The decline part in

the curve shows the effect of energy recovery. For contrast, we also draw the energy dissipation curve of the common two stage inverter using DC power supply with the same conditions. It is shown that the former circuit has about 86% of energy saving in comparison with the latter. The power saving is remarkable.

Based on the basic clocked CMOS inverter shown in Fig.2(a), we can realize NOR, NAND functions by using switches in series and parallel, then the clocked CMOS circuits with more complicated logic function may be achieved.

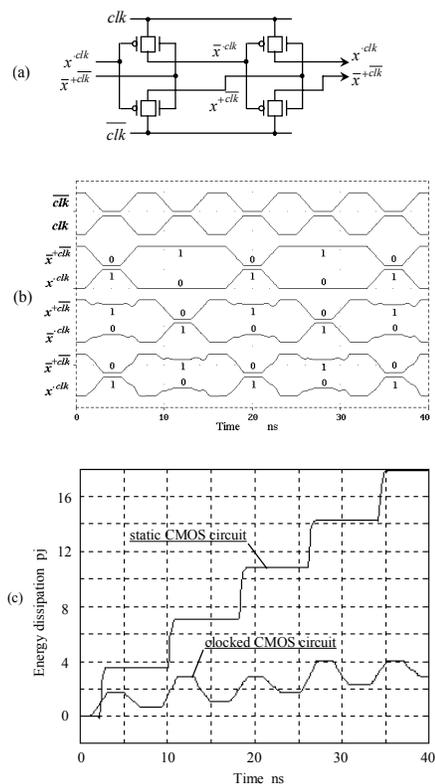


Figure 2. Clocked CMOS gate using a trapezoidal power-clock (a) circuit, (b) output waveforms, (c) energy dissipation curve.

IV. Clocked CMOS flip-flop

In the previous section we found that the signal at each node is fixedly set to base-0 or base-1 when $clk = 0$. In this way, a signal never be stored in this period. Thus, we cannot build a flip-flop by simply using gates as usual.

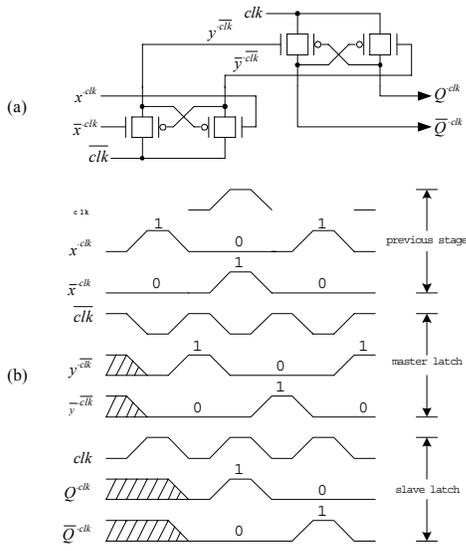


Figure 3. (a) Clocked CMOS base-0 flip-flop, (b) timing waveforms

Reference [9] presents a memory cell with “master-slave” structure, as shown in Fig.3(a). We first discuss the working process of the master latch by referring the waveforms shown in Fig.3(b). The inputs of the master latch are a pair of logic complementary base-0 signals $x^{\cdot clk}$ and $\bar{x}^{\cdot clk}$. their input sequences are supposed being 101... and 010.... The power clock of the master latch is \overline{clk} which differs from clk used to generate $x^{\cdot clk}$, $\bar{x}^{\cdot clk}$ in the previous stage. Therefore, the two outputs $y^{\cdot clk}$ \square $\bar{y}^{\cdot clk}$ are set to “base” when $\overline{clk} = 0$, i.e. $clk = 1$, and their waveforms are delayed with respect to the inputs $x^{\cdot clk}$ \square $\bar{x}^{\cdot clk}$ by one-half the clock period. The similar discussion can be made for the slave latch with power clock clk in Fig.3(a). Therefore, the output $Q^{\cdot clk}$ \square $\bar{Q}^{\cdot clk}$ resume to set base when $clk = 0$. Because they lag one-half the clock period once more, they are just delayed with respect to the original inputs ($x^{\cdot clk}$ \square $\bar{x}^{\cdot clk}$) by one clock period, i.e. one-bit shifting. Based on the above discussion, the function of the clocked base-0 flip-flop shown in Fig.3(a) is corresponding to a traditional D flip-flop.

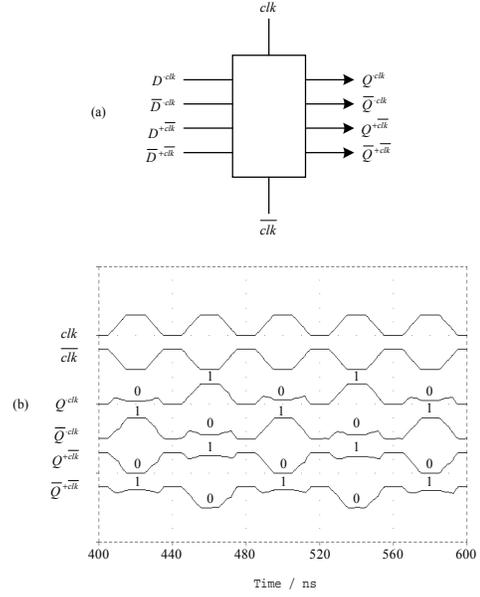


Figure 4. (a) Complete clocked flip-flop, (b) waveform of a modulo-2 counter

On the other hand, if we replace the pMOS transistor in the cross connection in Fig.3(a) with nMOS transistor, the clocked base-1 flip-flop will be built, where the inputs are x^{+clk} \square \bar{x}^{+clk} , and the outputs are Q^{+clk} \square \bar{Q}^{+clk} . We can build a complete clocked CMOS flip-flop by combining the clocked base-0 flip-flop with the clocked base-1 flip-flop, then its inputs and the outputs have all the four clocked signal types. Furthermore, based on the discussion in the previous section, four transmission gates can be attached to the outputs for restoration, as a buffer. We can use a legend shown in Fig.4(a) to represent the clocked CMOS flip-flop. If the four outputs $Q^{\cdot clk}$ \square $\bar{Q}^{\cdot clk}$ \square Q^{+clk} \square \bar{Q}^{+clk} are fed back to the inputs \square $\bar{D}^{\cdot clk}$ \square $D^{\cdot clk}$ \square \bar{D}^{+clk} \square D^{+clk} correspondingly, a modulo-2 counter is realized. The PSPICE-simulation result shown in Fig.4(b) indicates that the modulo-2 circuit has correct logic function. The further power analysis proved that the circuit has the advantage of low power. Based on the clocked CMOS flip-flop complex sequential circuits can be designed.

V. Conclusions

Clocked CMOS circuits, which adopt gradually rising and falling power-clock, can result in a considerable energy saving. However, the demand that the output signal should track the power-clock's gradually rising and falling behavior during charging and discharging makes the circuit design even difficult. At present, the existing researches either adopt retractile cascade power clocks or use multiple phase power clocks with memory schemes in the design. The problem is: the applicability of the designed clocked circuits is awfully limited. We think that the research on algebra expression of clocked signals and the design of basic clocked gates are two key researches. Therefore, this paper firstly presents a systematic study of clocked signals using an appropriate algebra expressions, and fully exploits the four types of clocked signal. Furthermore, some clocked CMOS gate circuit based on transmission gate are proposed. The clocked transmission gate supplied with a trapezoidal power clock was simulated with PSPICE and demonstrated to have correct logic function and considerable energy saving. The design principle can also be extended to design more complicated clocked CMOS circuits. If the clocked CMOS flip-flops are compounded, the design of low power clocked CMOS sequential circuits can be realized.

Acknowledgments

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