Referee: 2 Baranov
Detailed comments

-- No comments

Referee: 54 Steinbach
Detailed comments
shorten the paper especially the introduction explain the influence of faults outside of the Progammable AND Plane

-- We removed the influence of faults outside of the Progammable AND Plane and made introduction short.

Referee: 27 Selvaraj
Detailed comments
The paper could be shortened. For example, the introduction is too long and elaborates on points that are obvious.
The paper deals with a very important and appropriate topic. It presents some inovative methods to design for testability and self-repair.

-- We made introduction short and removed elaborates on points that are obvious.

Referee: 55 Krasniewski

Detailed comments
General remarks:
1. The paper presents an interesting idea of using a universal test set to detect and locate cross-point faults in a GAL device and an
implementation of a self-repairable device which uses this set.

-- No comments

2. The major technical problem with the paper relates to the fault model. Although I agree that crosspoint faults, called cross-point stuck-at faults by the Authors, are most common in programmable devices, there are some other faults - like bridging faults (typically considered in papers on PLA testing) which are quite likely to occur in GALs. Also, there might be some physical defects that are difficult to represent by any commonly used fault model. Therefore, the results of the failure rate analysis presented in the paper are questionable. They are only valid under assumption that all physical defects that can occur in a GAL device are adequately represented by the assumed stuck-at fault model. However, as mentioned earlier, this assumption does not hold.

-- We put your comment, "The results of the failure rate analysis are only valid under assumption that the assumed stuck-at fault model adequately represents all physical defects that can occur in a GAL device," in the evaluation section (page 13).

3. The submission is too long for a journal paper. The Authors go too much into details. Some parts are strictly commercial (evaluation of the PLD market on page 1),

-- This citation was removed.

Other statements are not related to the topic of the paper (e.g. because of the assumed model of the system architecture - section 3.2 - a discussion on page 1 on using PALs and GALs in VLSI chips is irrelevant).

-- This paragraph was removed.

Also, the list of references is too long.

-- Now, we have 26 references (previous one had 39 references).

Details:

1. I have difficulties in interpreting the considered values of the failure rates. Why are they expressed in percentages? Does this comply with the definition of FIT given in the paper?

   -- The PPM, 0.05% was obtained roughly from 489 defective devices among 10,000 devices, and the FIT, 5.00% was provided approximately from 5.07% to simplfy number (page 13).
   -- Originally, the PPM is presented by defective devices per 10,000 devices, and the FIT is presented by defectived percentage.

2. The measure of performance defined in section 5 is perhaps unfortunate. For illustration purposes you can calculate the ratio of looping time and area overhead, but if you say 'performance' one could expect to see some indicators of speed, power consumption etc. By the way, your design leads to non-negligible increase in power consumption and perhaps also to some speed degradation (larger circuits implementing a given function are usually slower).

   -- Dr. Hall will help those question...
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3. The statement on very (!) good coverage of physical defects in CMOS circuits by the stuck-at fault model (page 5) is a significant exaggeration.

   -- We remmoved a word, “very” in this sentence. It was refered to many references.This sentence could be removed.