WHAT IS THIS CLASS ABOUT?

DESIGN OF VLSI CIRCUITS

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Stanford University

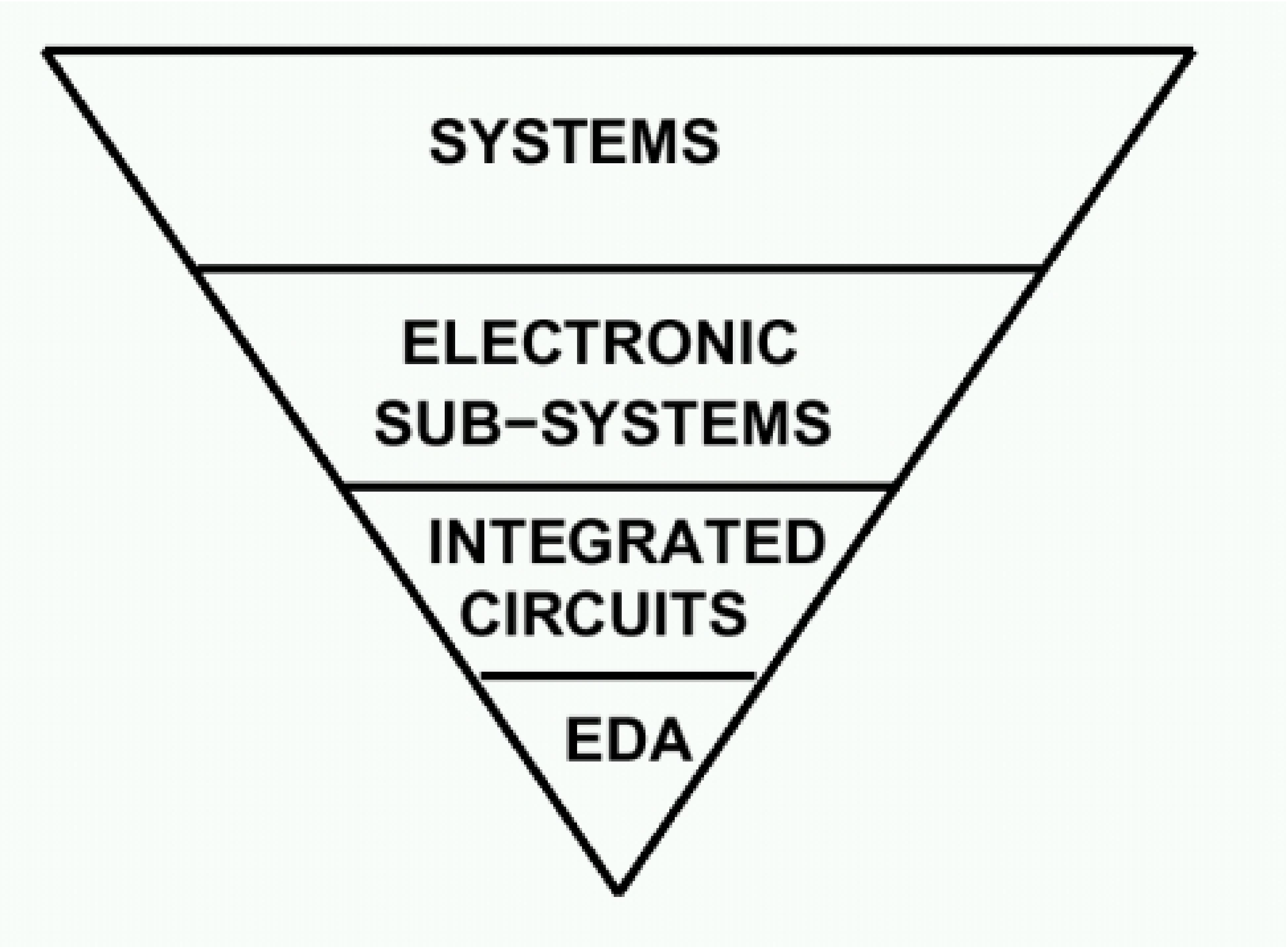
Microelectronics

- Enabling and strategic *technology*.
- Primary markets:
  - Information systems.
  - Telecommunications.
  - Consumer.
- Secondary markets:
  - Systems (e.g., transportation).
  - Manufacturing (e.g., robots).
- Application of VSLI circuit technology.

Computer-Aided Design

- Enabling design *methodology.*
- Makes electronic design possible:
  - Large scale design management.
  - Design optimization.
  - Reduced design time.
- Key strategic importance.

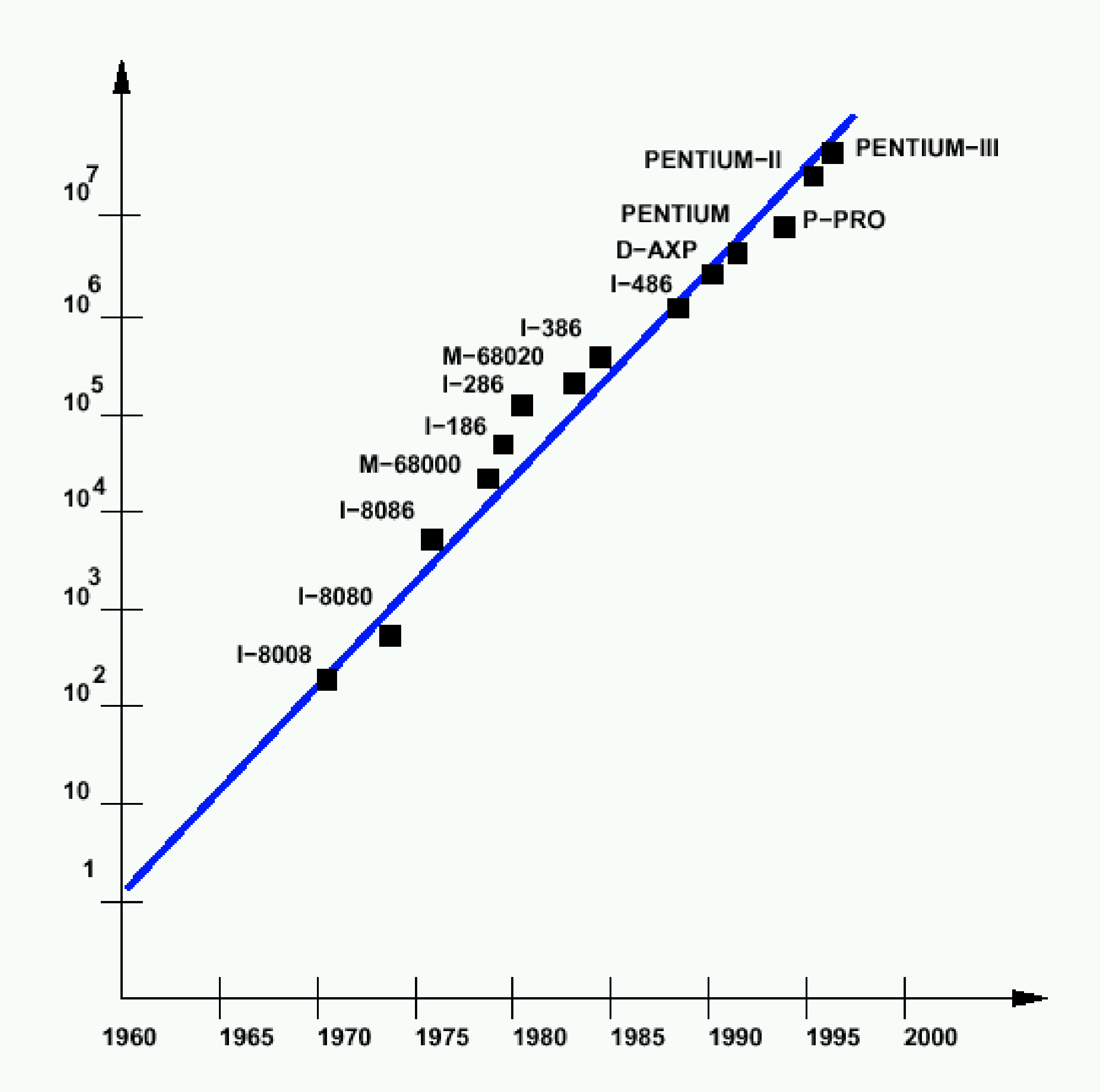
Electronic market



Trends in microelectronics

- Improvements in device technology:
  - Smaller circuits.
  - Higher performance.
  - More devices on a chip.
- Higher degree of integration.
  - More complex systems.
  - Lower cost of computation.
  - Higher reliability.

Moore's law



PENTIUM-III
PENTIUM-II
PENTIUM
P-PRO
D-AXP
I-486
I-386
M-68020
I-286
I-186
M-68000
I-8086
I-8080
I-8008
10^7
10^6
10^5
10^4
10^3
10^2
10
1
1960
1965
1970
1975
1980
1985
1990
1995
2000

Integration-scale limitations

- Intrinsic physical scaling limits.
- Capital investment for fabrication.
  - Use of appropriate design styles.
- Large-scale design management.
  - Use of CAD design tools.

Microelectronic design problems

- Use most recent technologies.
  - To be competitive in performance.
- Reduce design cost.
  - To be competitive in price.
- Speed-up design time.
  - Time-to-market is critical.

Microelectronic economics

- Design cost:
  - *Design time* and ***fabrication cost***.
  - Large ***capital investment***.
  - Near impossibility to *repair.*
- Recapture costs:
  - Large ***volume*** production is beneficial.
  - ***Zero-defect*** designs are essential.
  - Follow market ***evolution.***

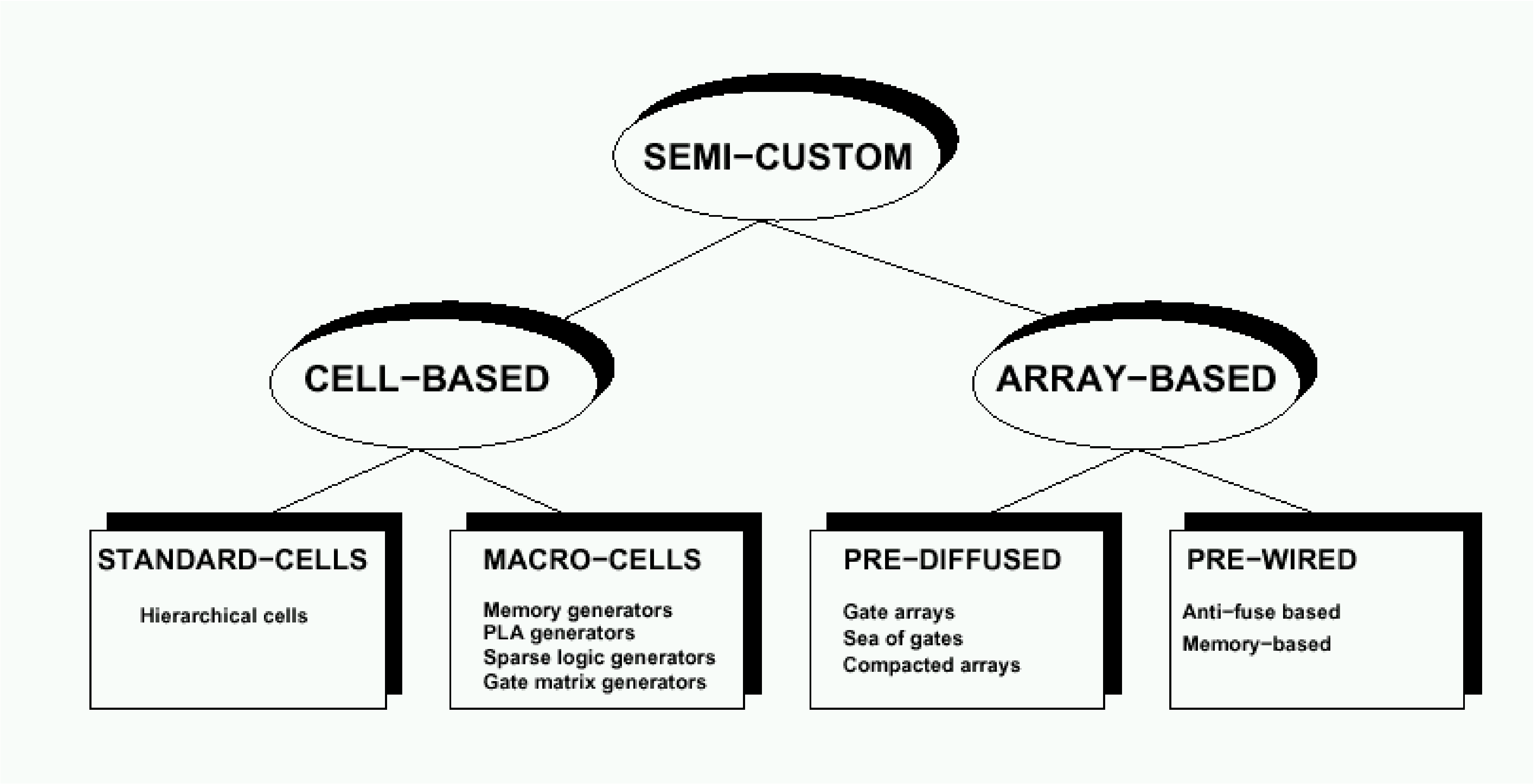
Microelectronic circuits

- General-purpose processors:
  - High-volume sales.
  - High performance.
- Application-Specific Integrated Circuits (ASICs):
  - Varying volumes and performances.
- Prototypes.
- Special applications (e.g. space).

Microelectronic design styles

- Adapt circuit design style to market requirements:
- Parameters:
  - Cost.
  - Performance.
  - Volume.
- Custom and semi-custom design.

Semi-custom design



Standard cells

- Cell library:
  - Cells are designed once.
  - Cells are highly optimized.
- Layout style:
  - Cells are placed in rows.
  - Channels are used for wiring.
- Compatible with macro-cells (e.g. RAMs).

Macro-cells

- Module generators:
  - Synthesized layout.
  - Variable area and aspect-ratio.
- Examples:
  - RAMs, ROMs, PLAs, general logic blocks.
- Features:
  - Layout can be highly optimized.
  - Structured-custom design.

Array-based design

- ***Pre-diffused*** arrays:
  - Personalization by metalization/contacts.
  - Mask-Programmable Gate-Arrays.
- ***Pre-wired*** arrays:
  - Personalization on the field.
  - Field-Programmable Gate-Arrays.

MPGAs

- Array of ***sites***:
  - Each site is a set of transistors.
- Batches of wafers can be pre-fabricated.
- Few masks to personalize chip.
- Lower cost than cell-based design.

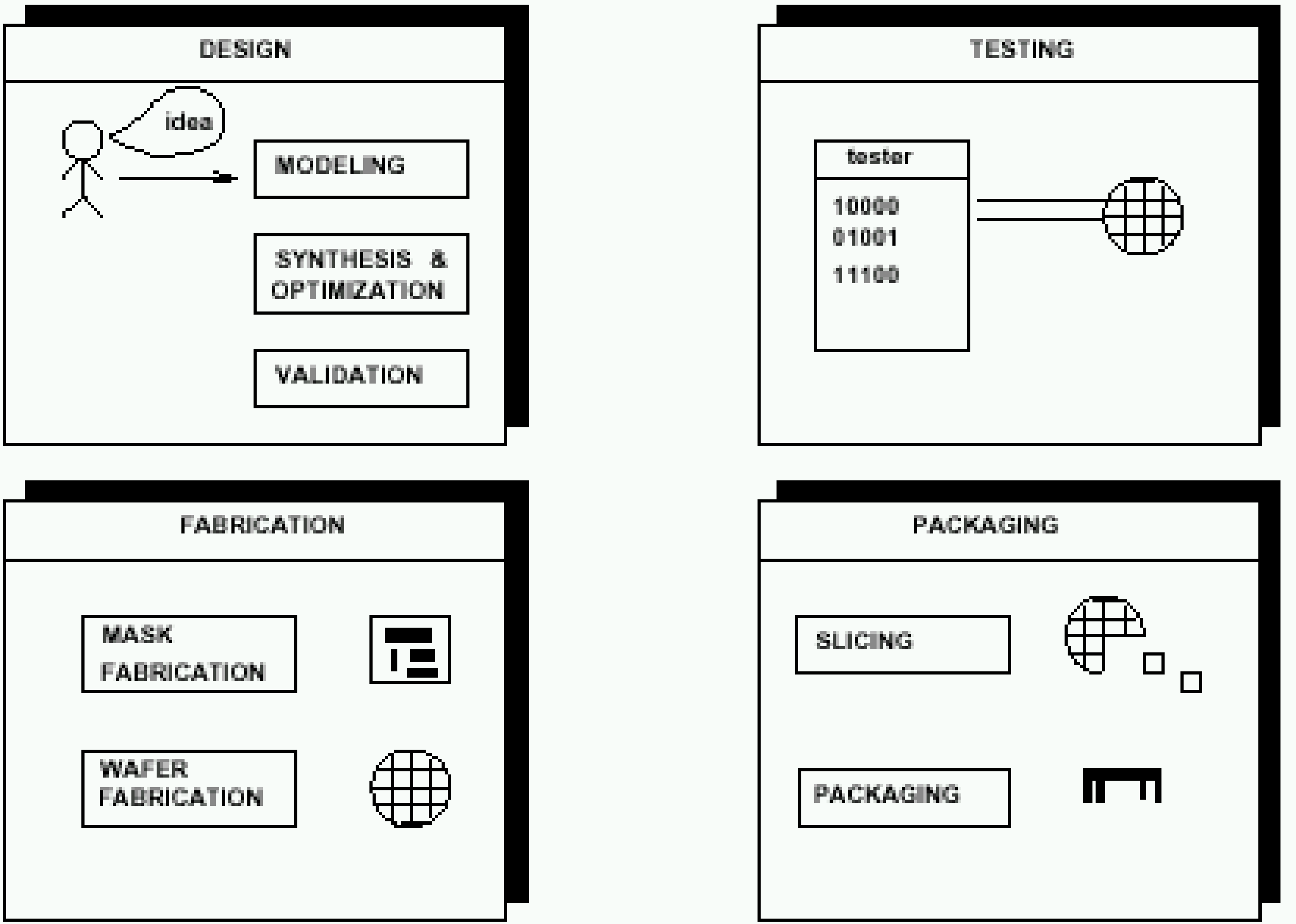
FPGAs

- Array of cells:
  - Each cell performs a logic function.
- Personalization:
  - Soft: memory cell (e.g. Xilinx).
  - Hard: Anti-fuse (e.g. Actel).
- Immediate turn-around (for low volumes).
- Inferior performances and density.
- Good for prototyping.

Semi-custom style trade-off

	Custom	*Cell-based*	*Pre-diff.*	*Pre-wired*
Density	Very High	High	High	Medium-Low
Performance	Very High	High	High	Medium-Low
Flexibility	Very High	High	Medium	Low
Design time	Very Long	Short	Short	Very Short
Man. time	Medium	Medium	Short	Very Short
Cost - lv	Very High	High	High	Low
Cost - hv	Low	Low	Low	Medium-High

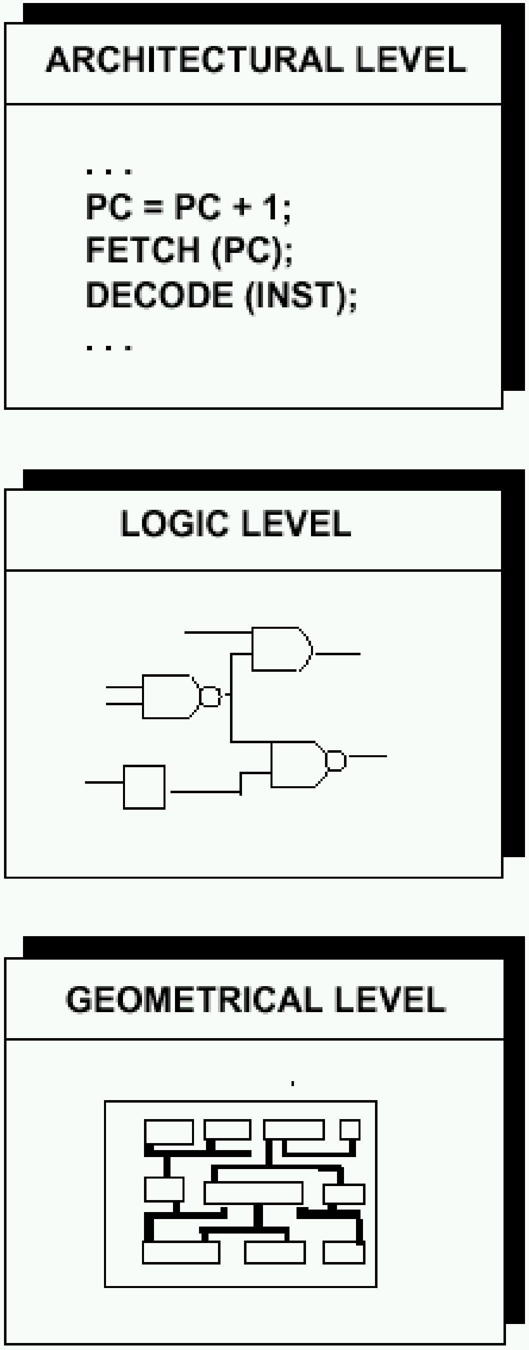
Microelectronic circuit design and production



Microelectronic circuit design

- Conceptualization and modeling:
  - Hardware Description Languages (HDLs).
- Synthesis and optimization:
  - Model refinement.
- Validation:
  - Check for correctness.

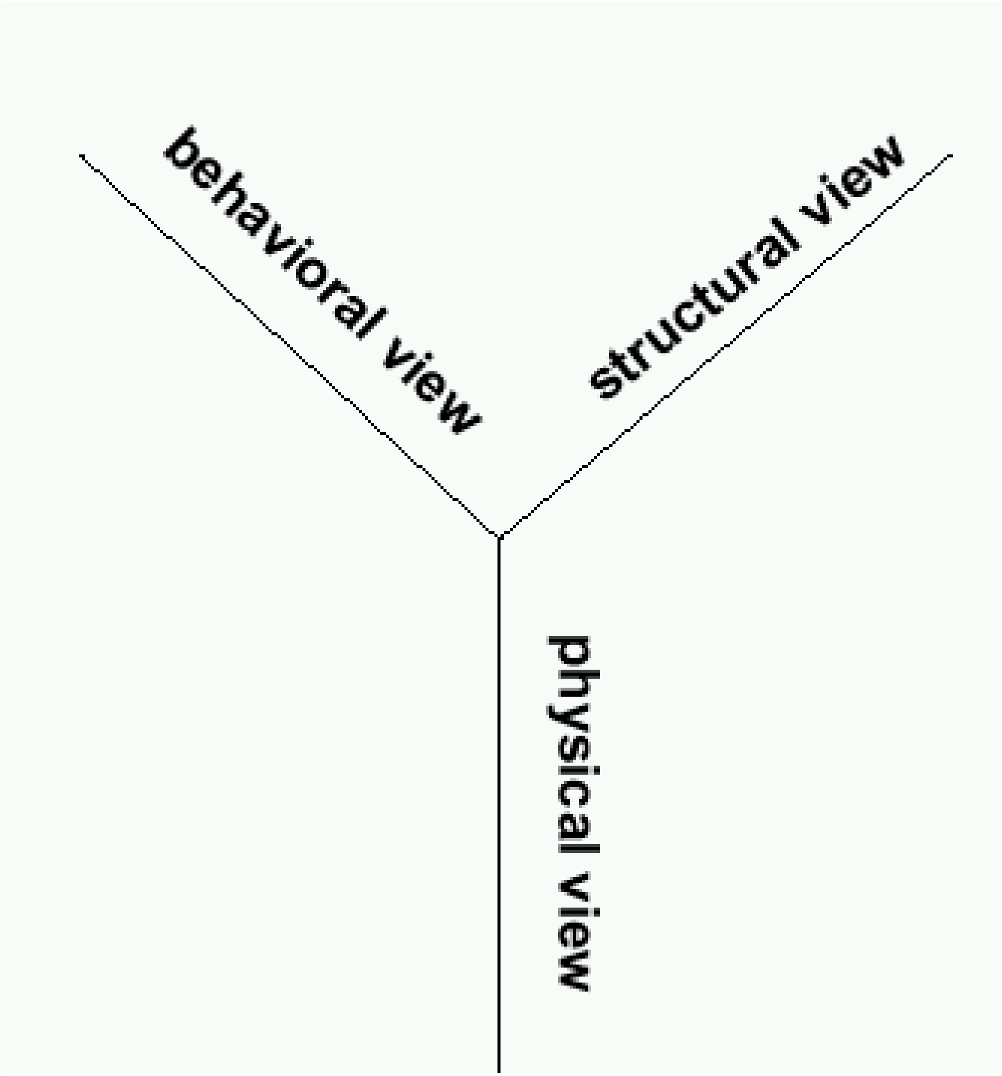
Modeling abstractions



Modeling abstractions

- **Architectural level:**
  - Operations implemented by resources.
- **Logic level:**
  - Logic functions implemented by gates.
- **Geometrical level:**
  - Devices are geometrical objects.

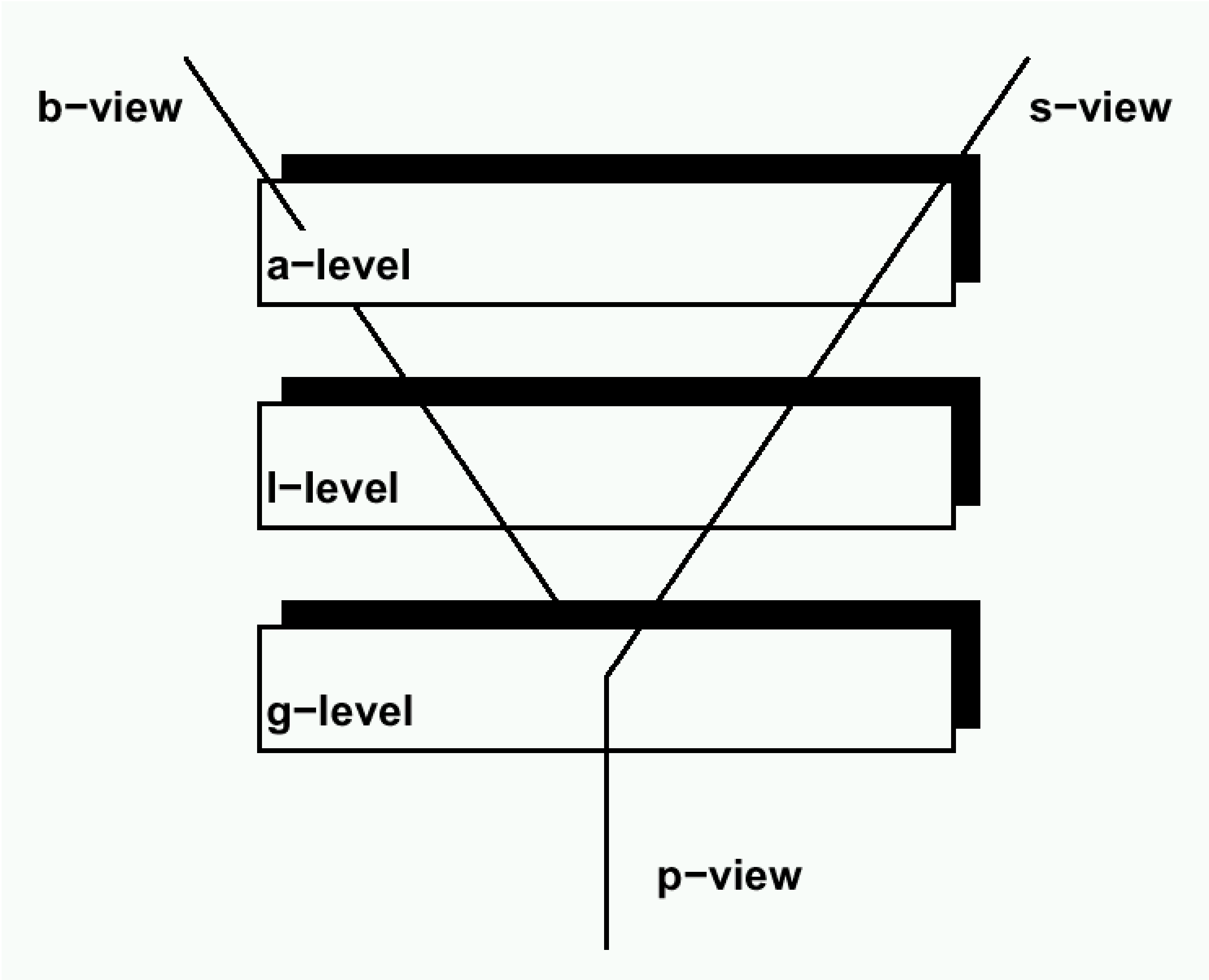
Modeling views



Modeling views

- Behavioral view:
  - Abstract function.
- Structural view:
  - An interconnection of parts.
- Physical view:
  - Physical objects with size and positions.

Modeling views and abstractions

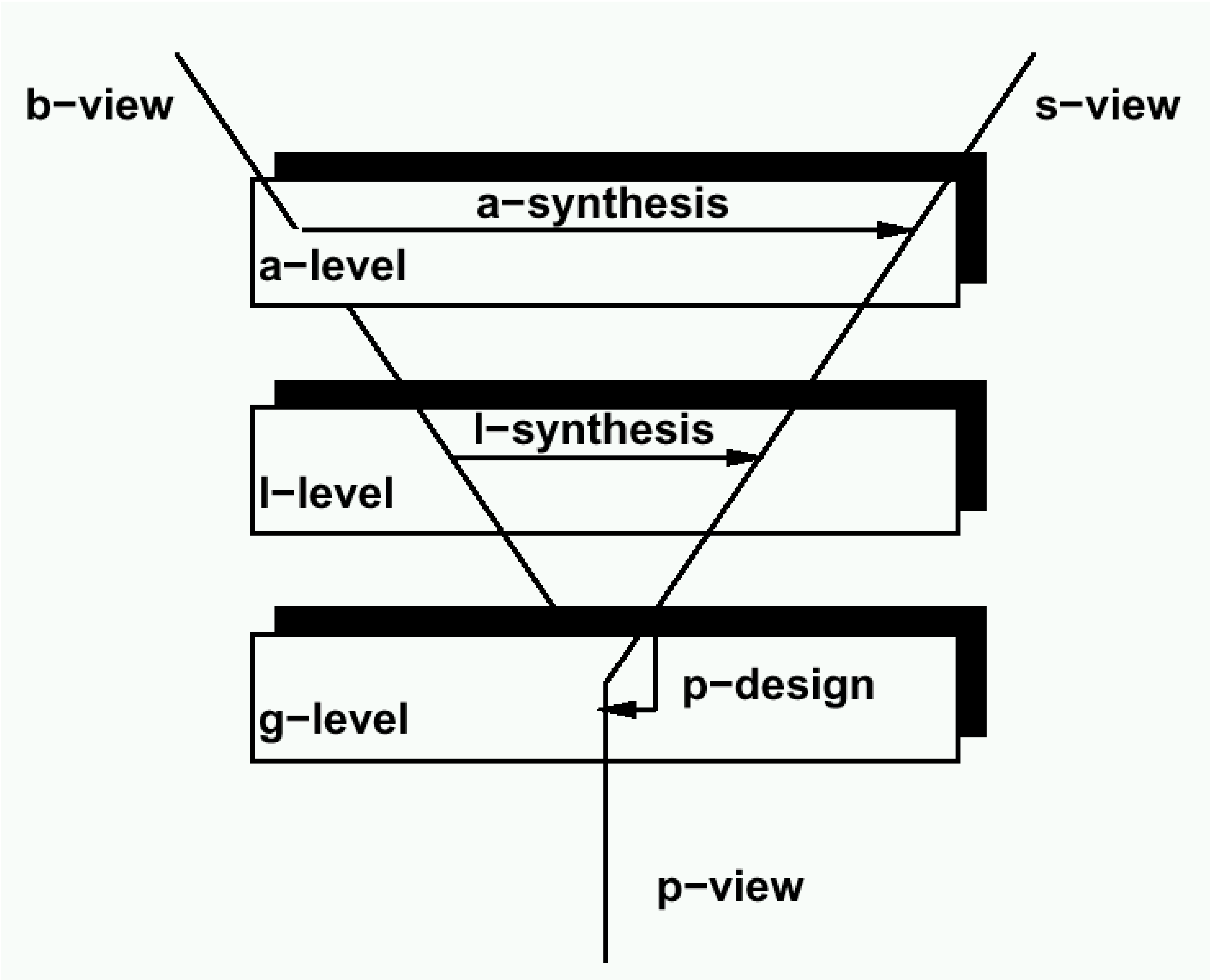


Circuit synthesis

- **Architectural-level synthesis:**
  - Determine the macroscopic structure:
    - Interconnection of major building blocks.
- **Logic-level synthesis:**
  - Determine the microscopic structure:
    - Interconnection of logic gates.
- **Geometrical-level synthesis:**

  (Physical design)
  - Determine positions and connections.

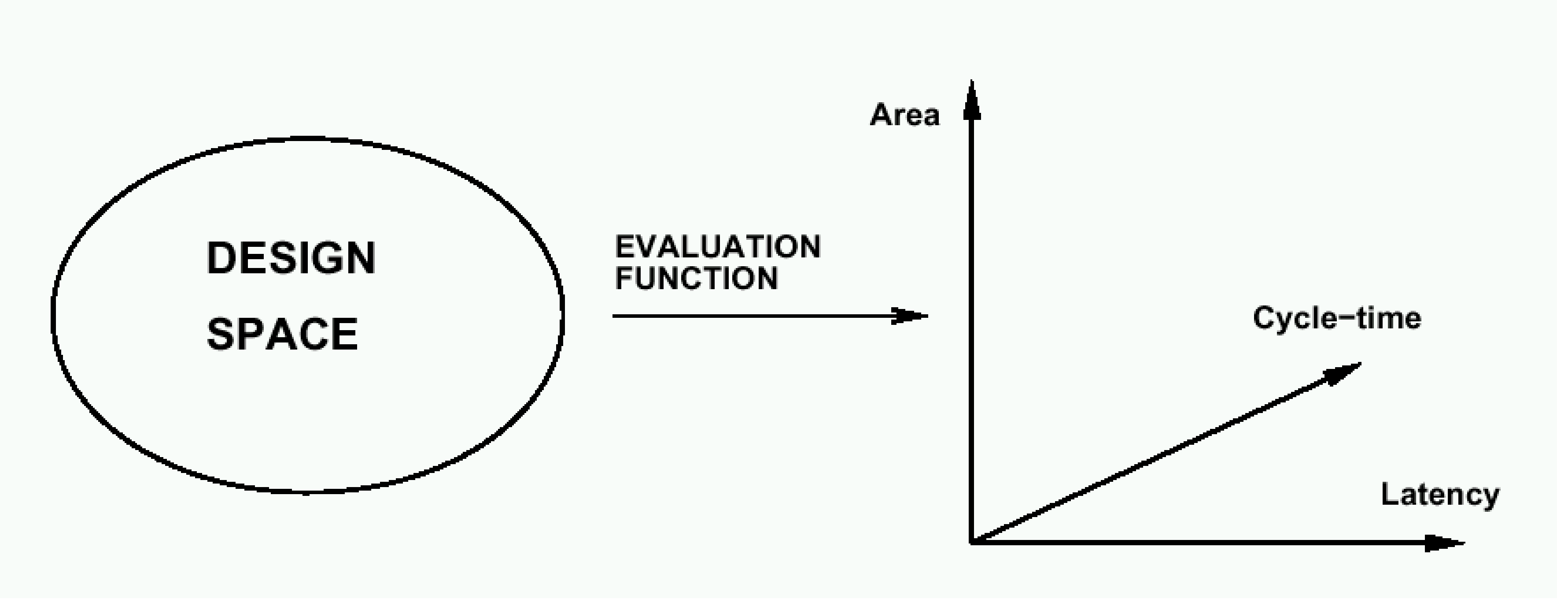
Modeling views



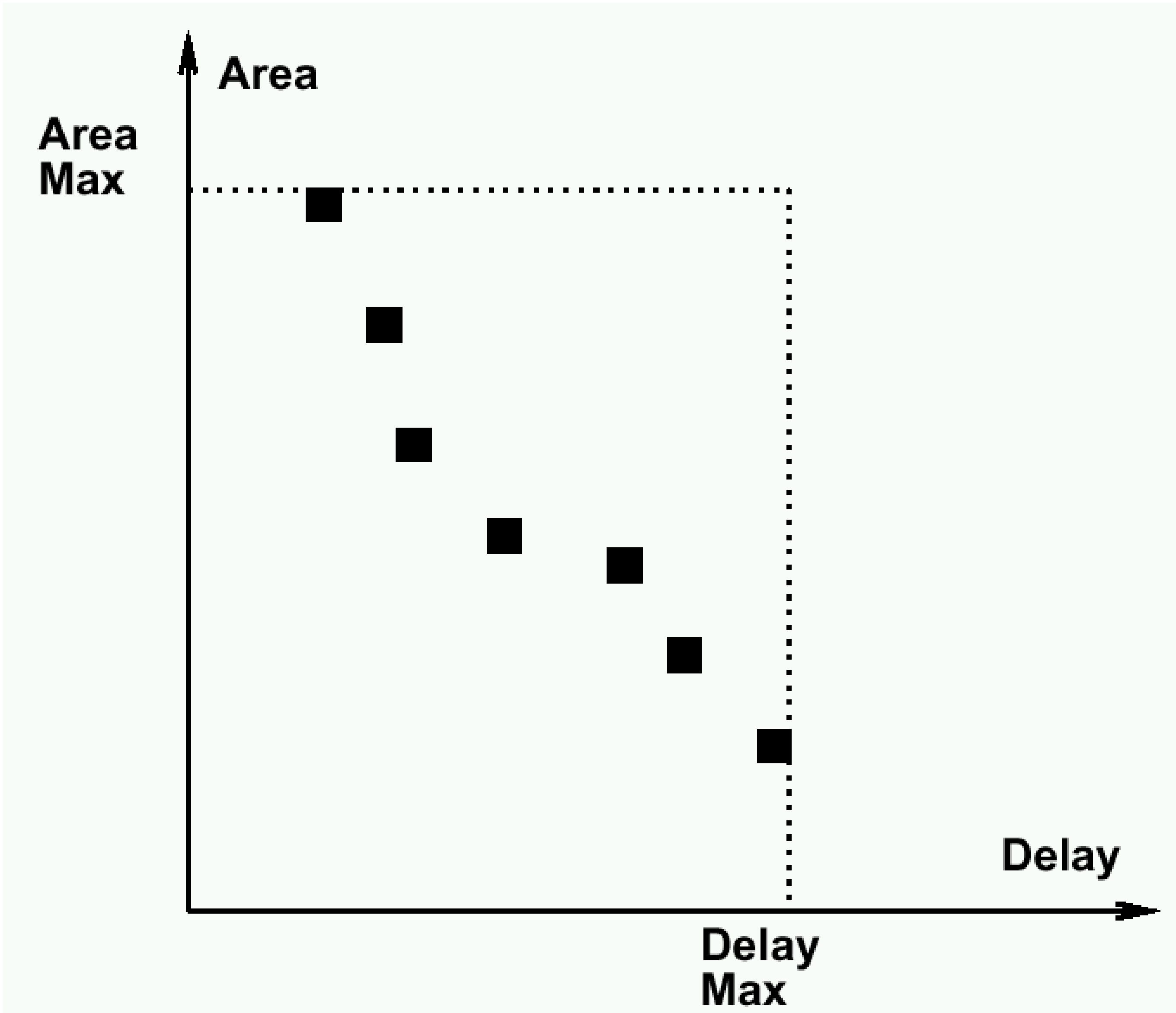
Microelectronic circuit optimization

- Performance:
  - Delay and cycle-time.
  - Latency.
  - Throughput (for pipeline applications).
- Power consumption.
- Area (yield and packaging cost).
- Testability.

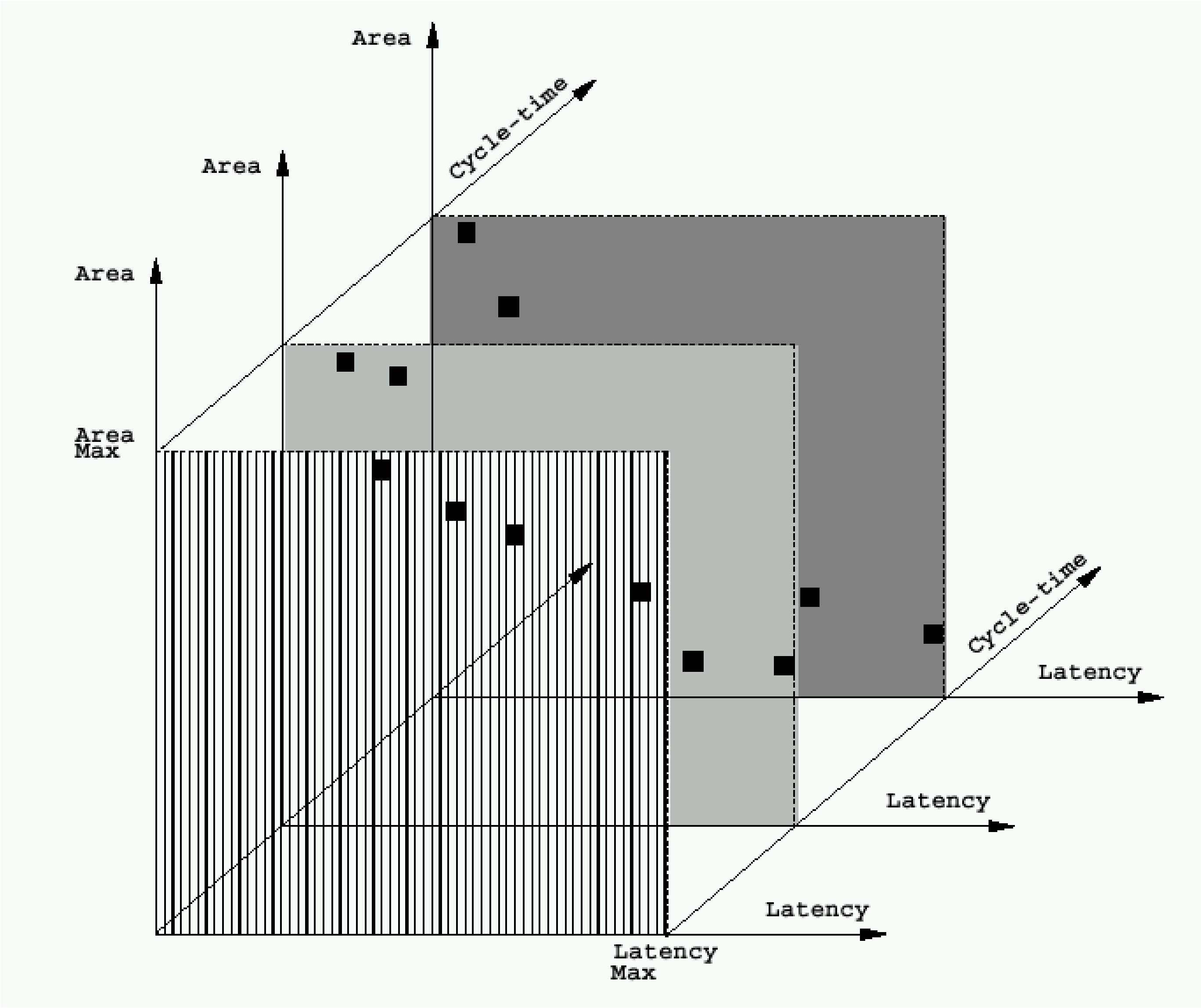
Design space and evaluation space



Optimization trade-off in combinational circuits



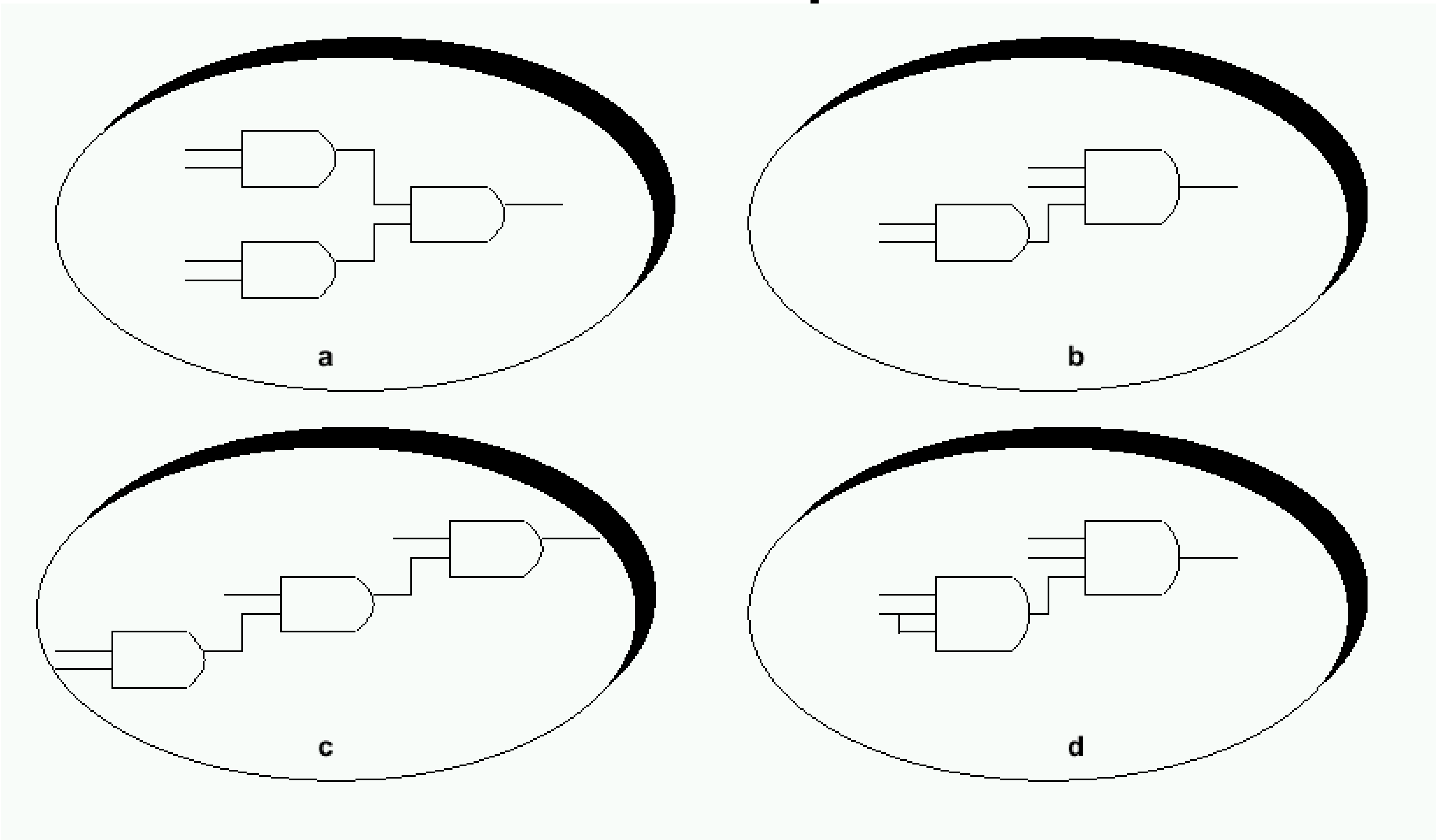
Optimization trade-off in sequential circuits



Pareto points

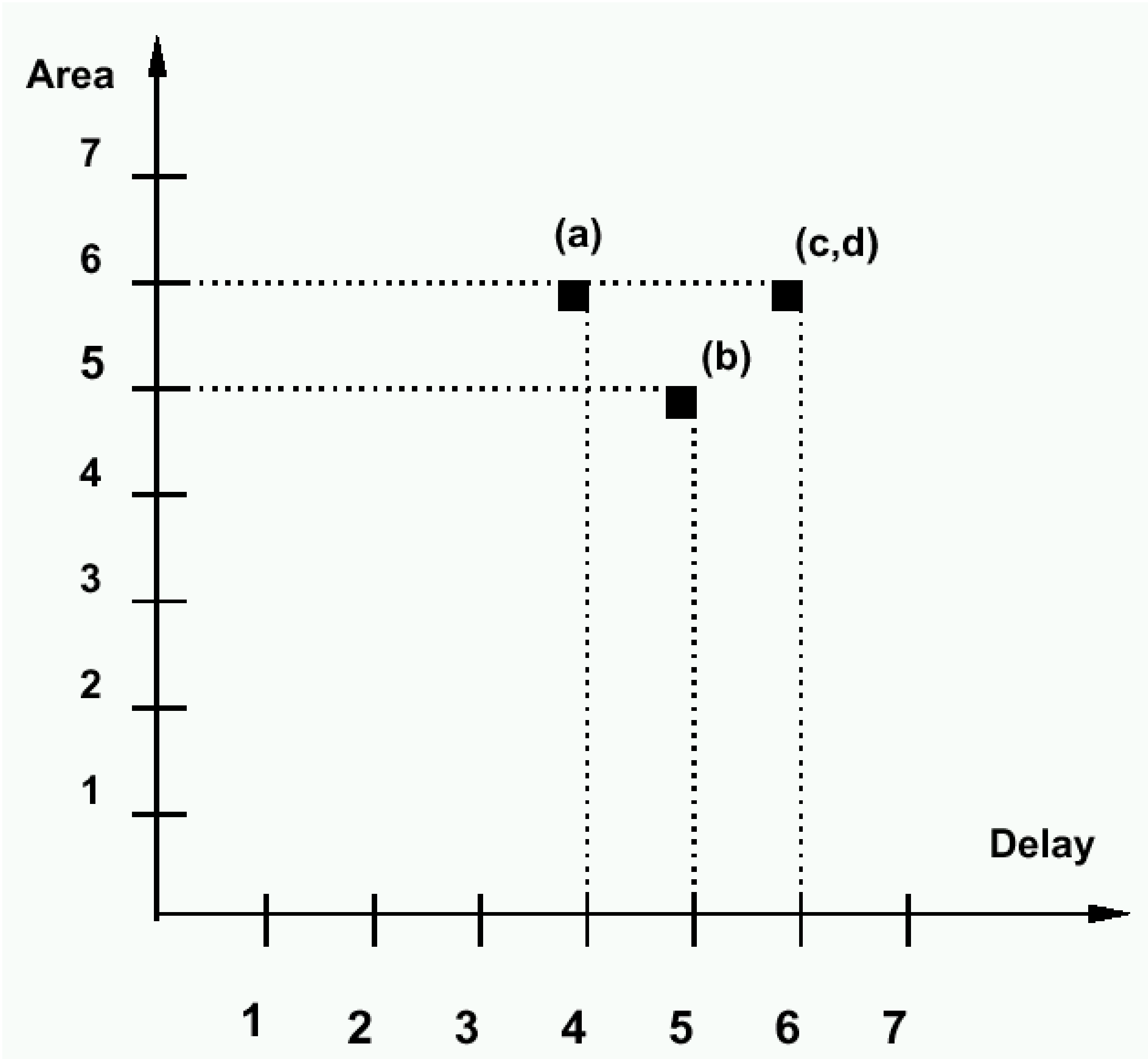
- Multi-criteria optimization.
- Multiple objectives.
- Pareto point:
  - A point of the design space is a Pareto point if there is <u>no other point with</u>:
    - at least one inferior objectives.
    - all other objectives inferior or equal.

Example



- **Implement** ***f = p q r s*** **with:**
  - **2-input or 3-input AND gates.**
- **Area and delay proportional to number of inputs.**

Example
design evaluation space



Summary

- Computer-aided design methodology:
  - Capture design by HDL models.
  - Synthesize more detailed abstractions.
  - Optimize circuit parameters.
- Logic synthesis and optimization:
  - Manipulate and optimize circuit models at the logic abstraction levels.