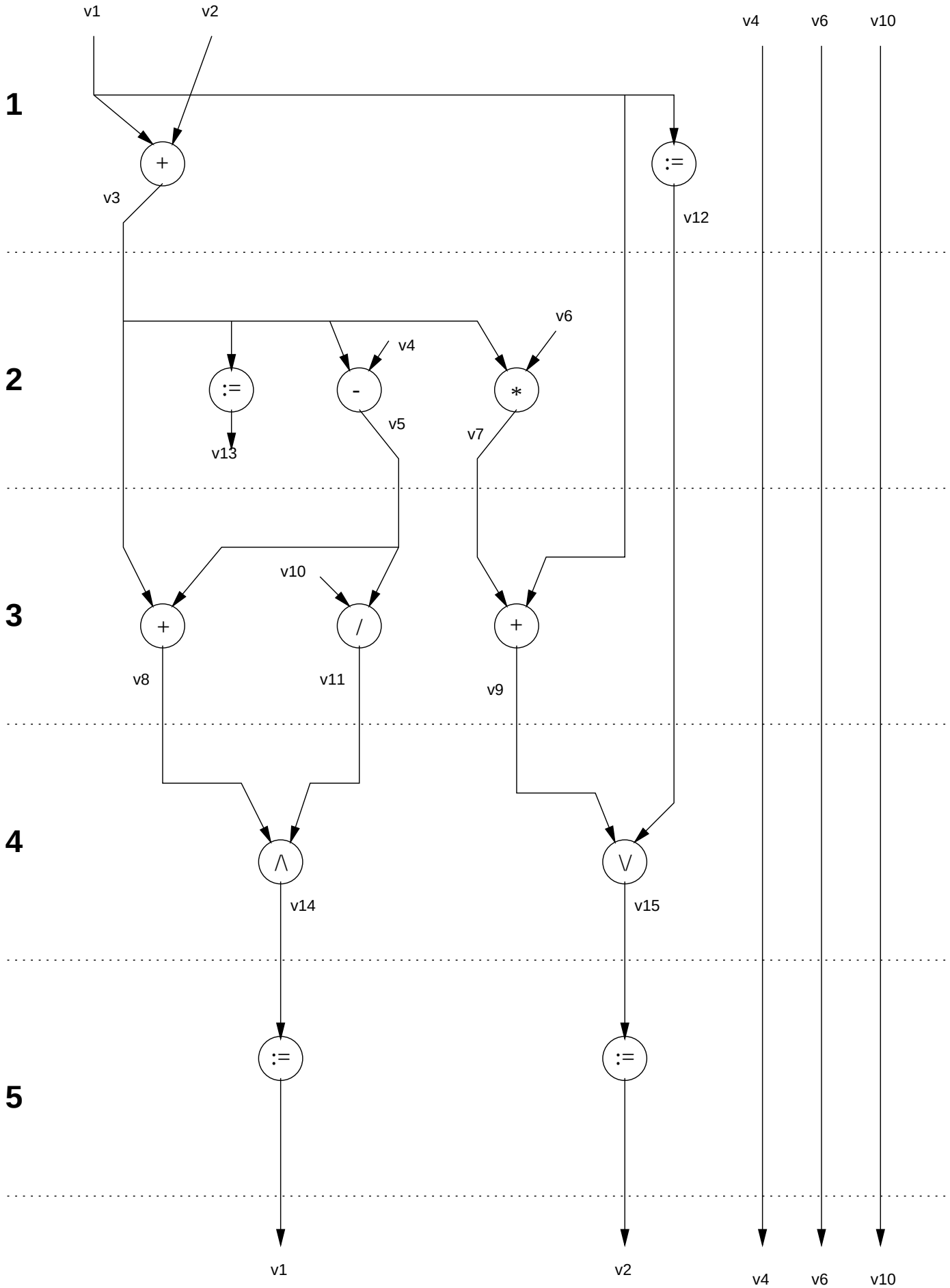
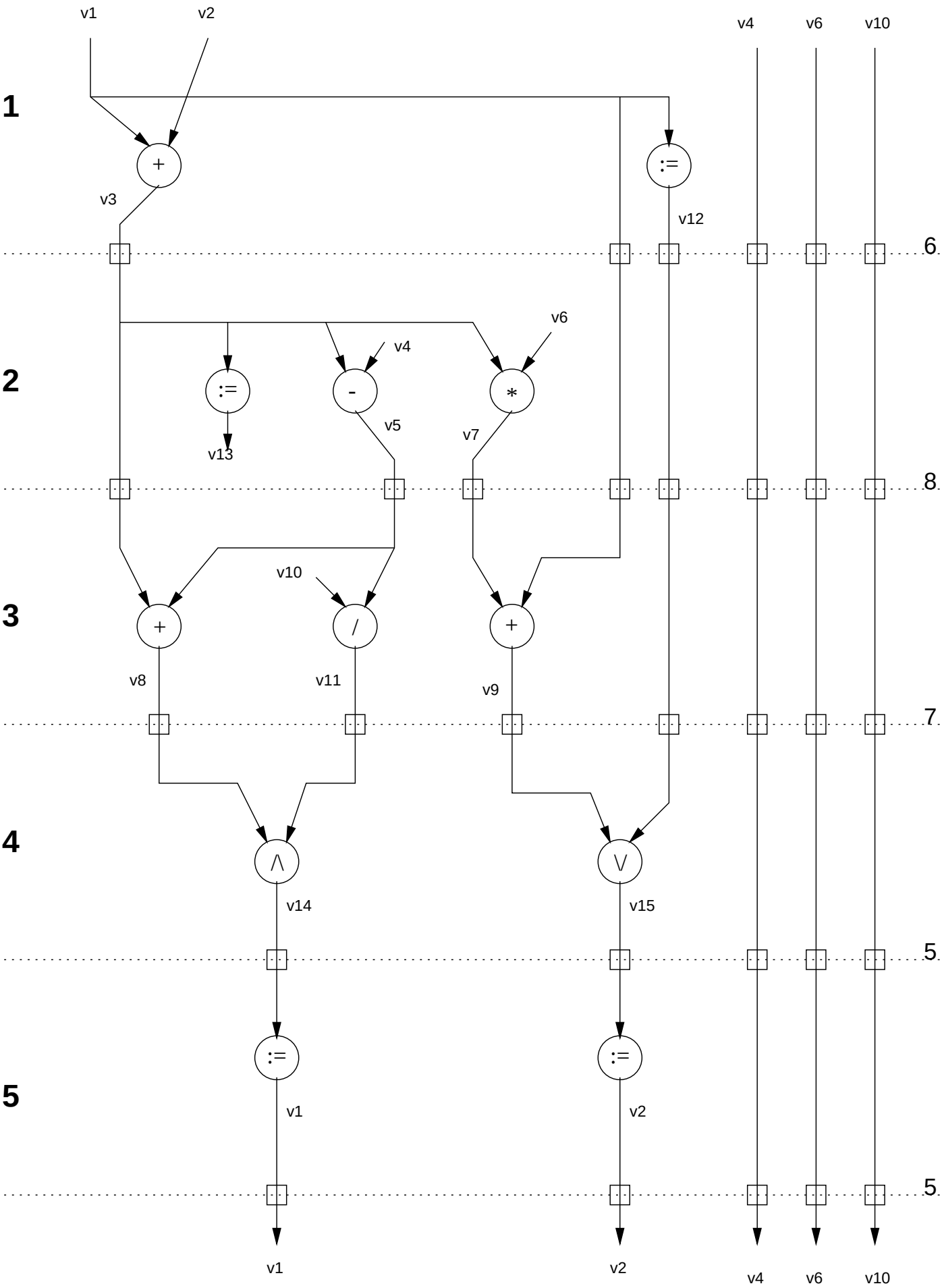
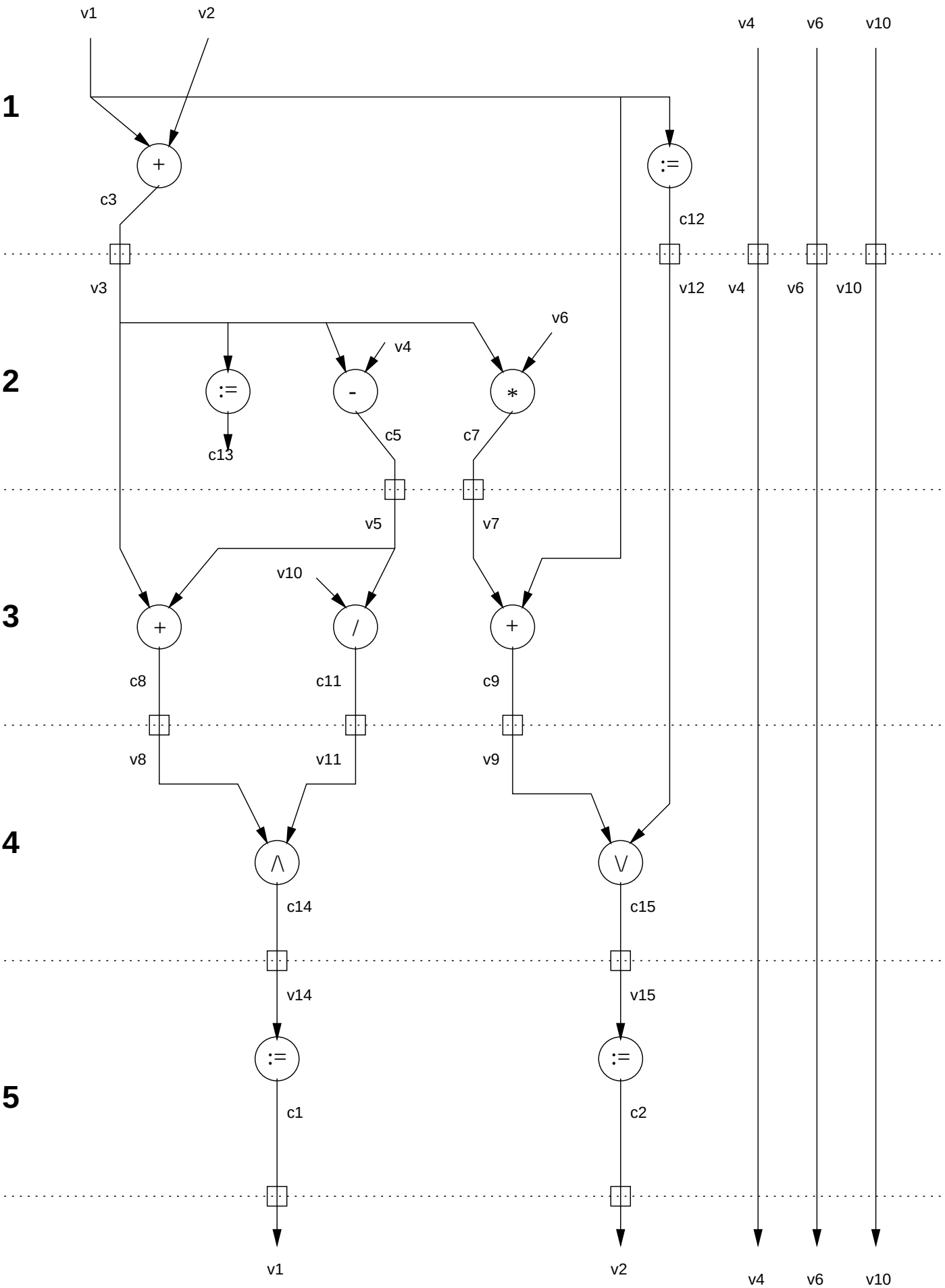


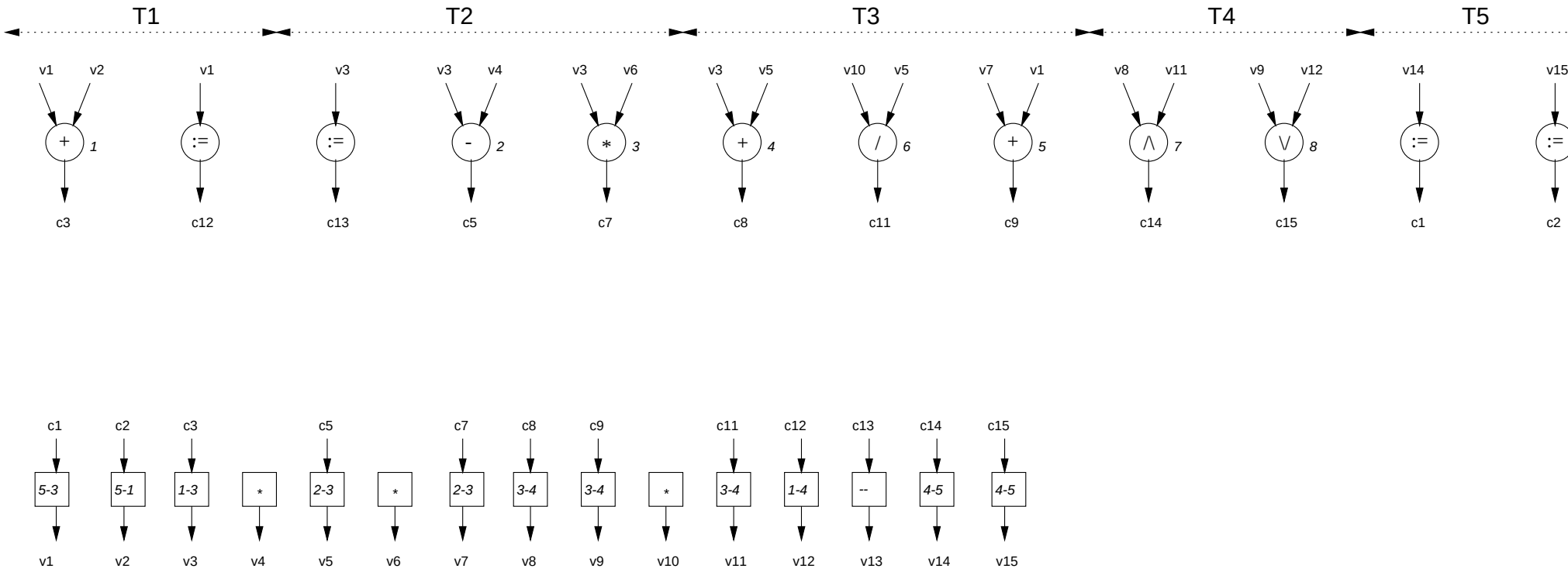
Allocation 1: Original scheduled data-flow graph



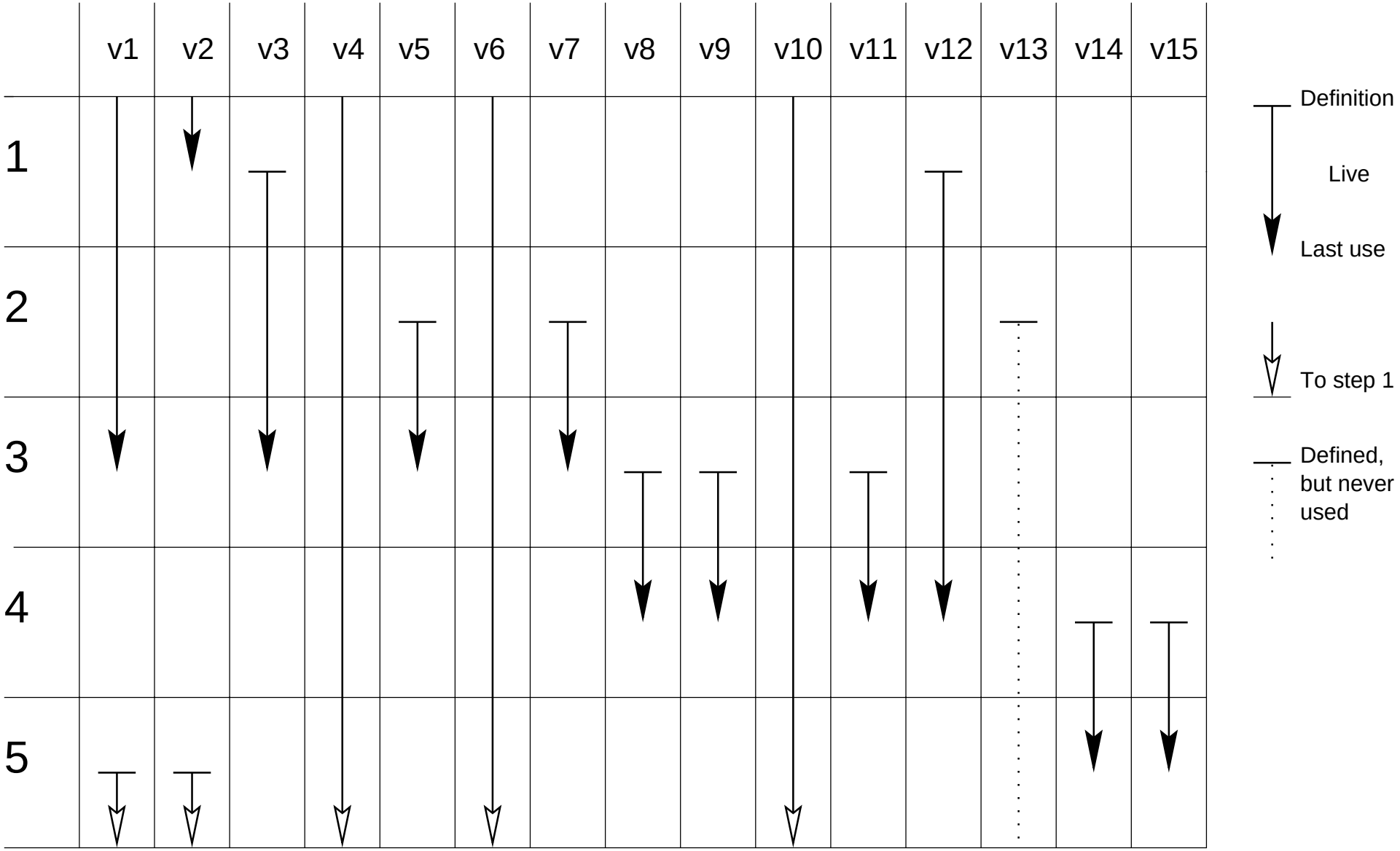
Allocation 2: Registers inserted

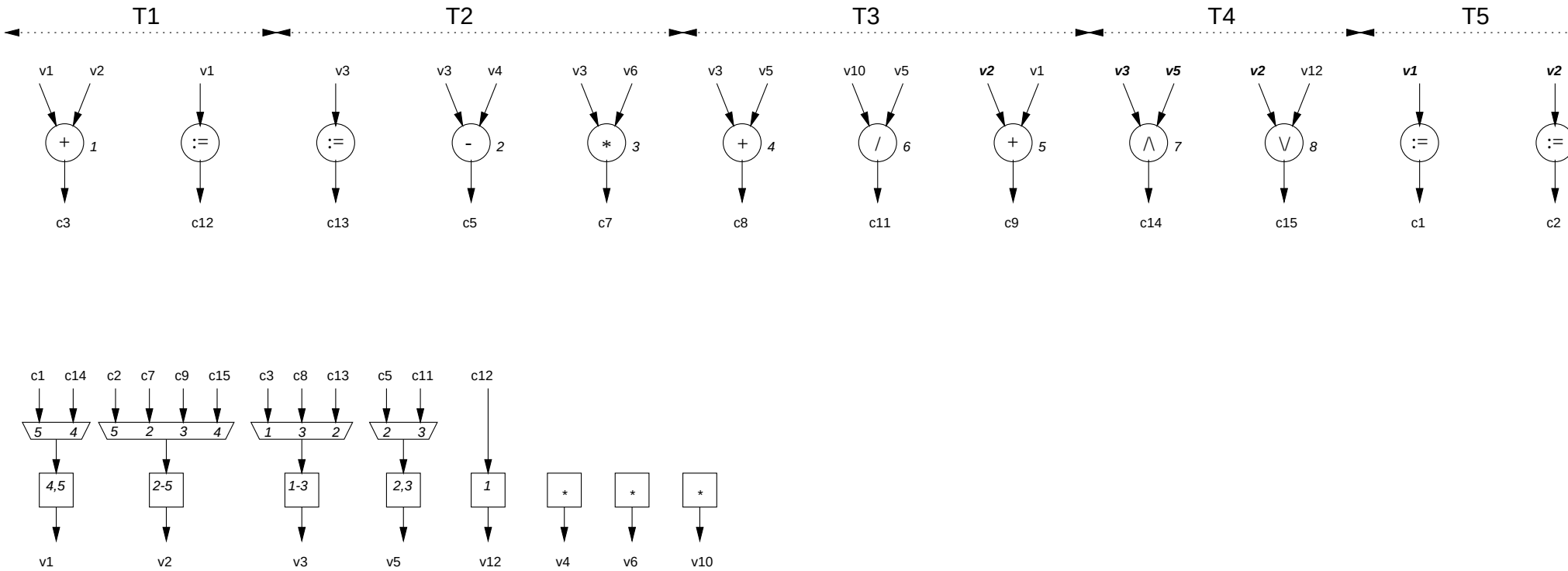


Allocation 3: Reduced number of registers

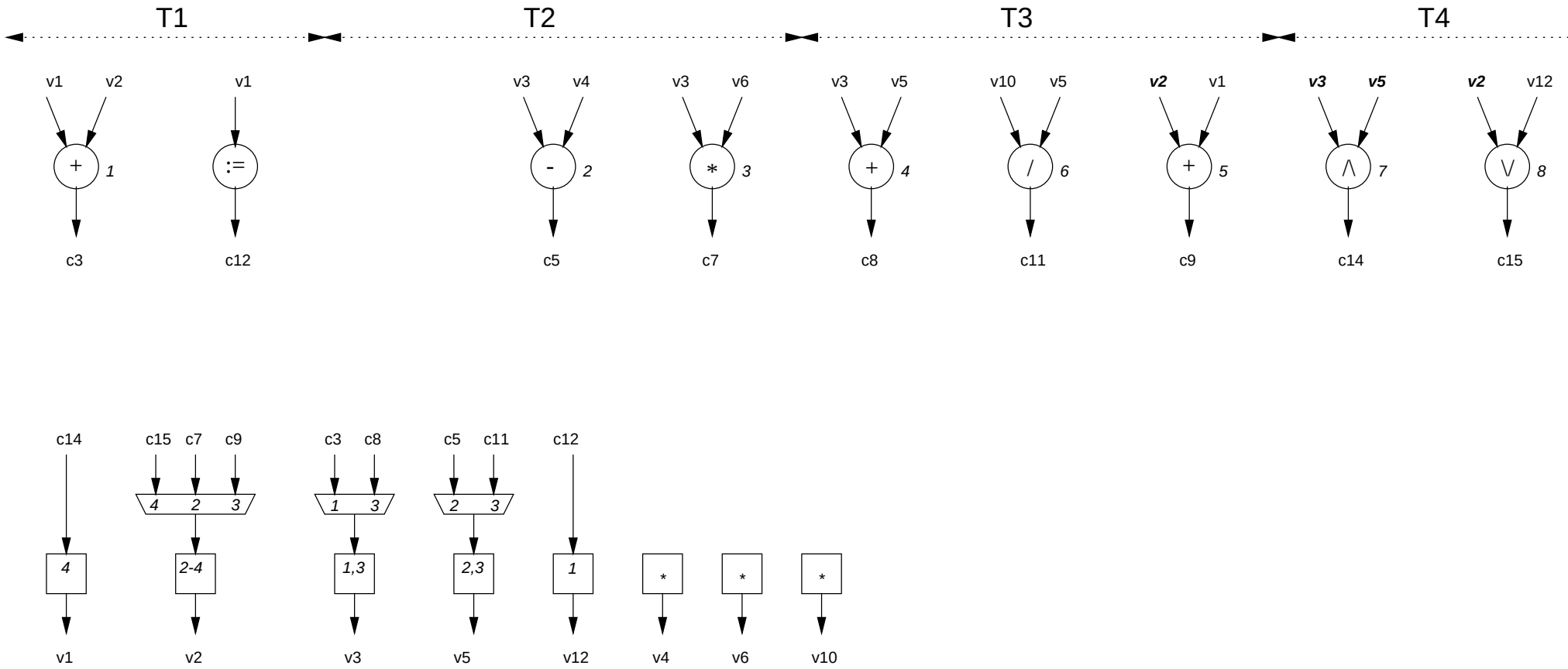


Allocation 4: Same picture as 3, but different layout

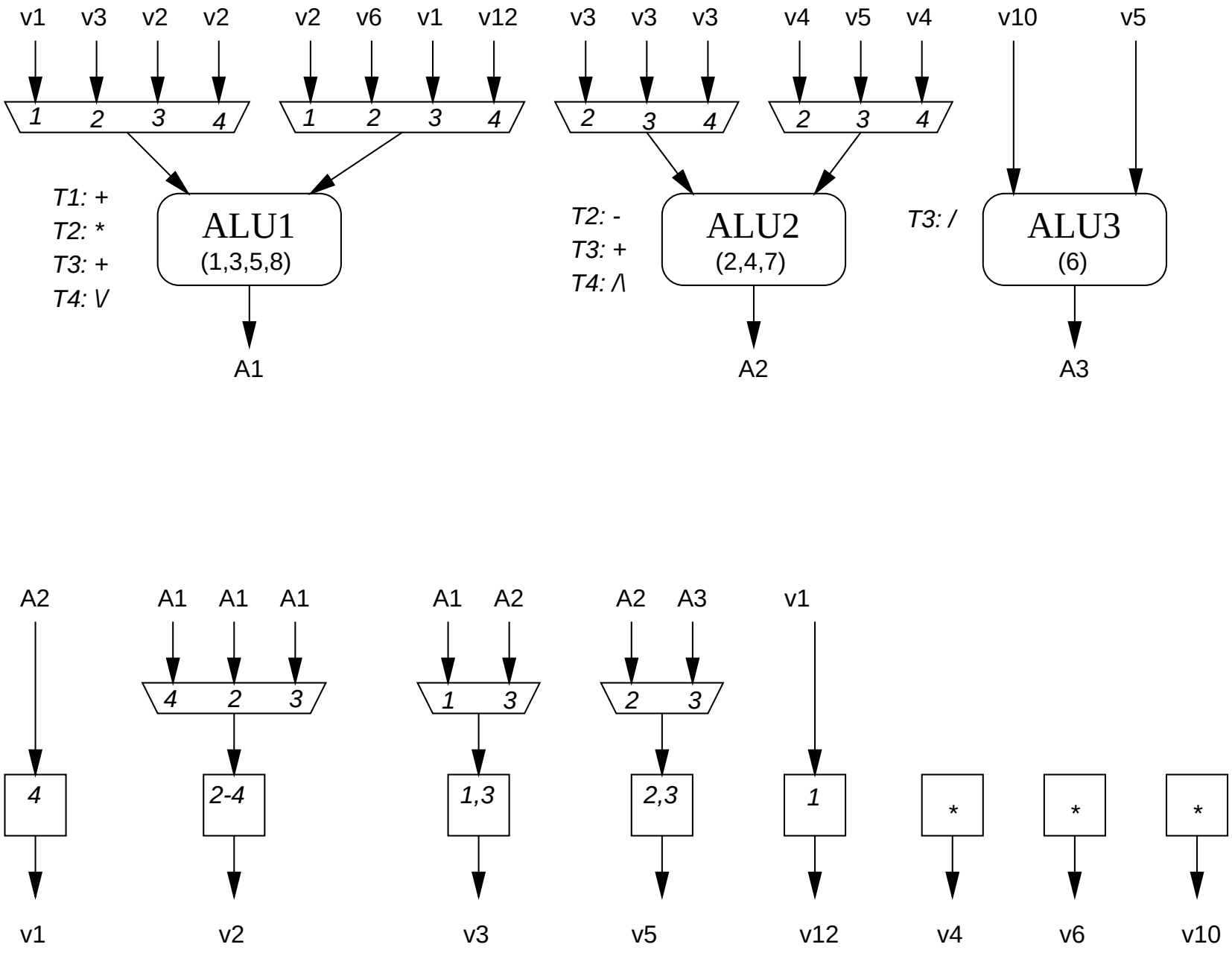

v1
v2
v3
v4
v5
v6
v7
v8
v9
v10
v11
v12
v13
v14
v15
1
2
3
4
5
Definition
Live
Last use
To step 1
Defined, but never used



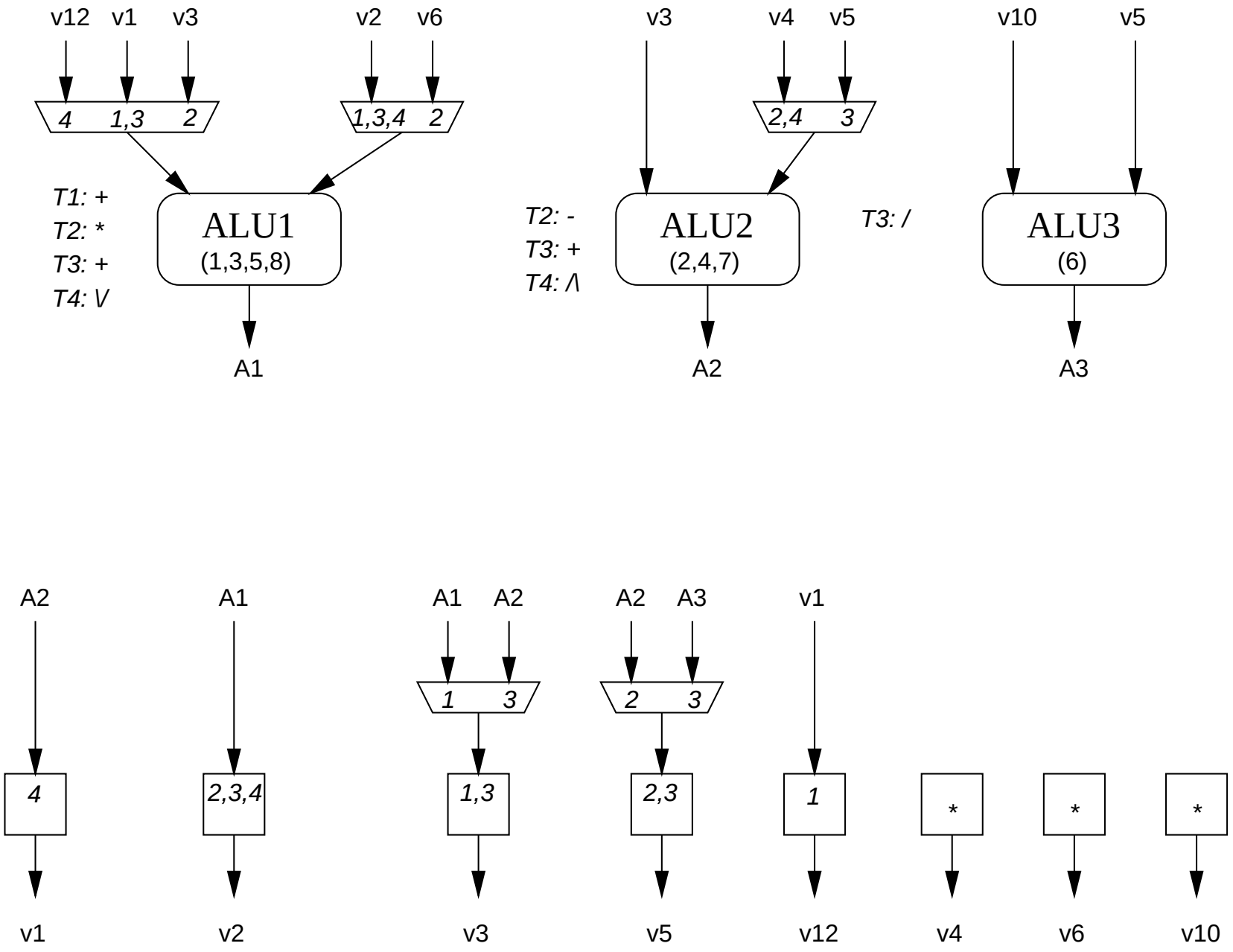
Allocation 5: Registers optimized



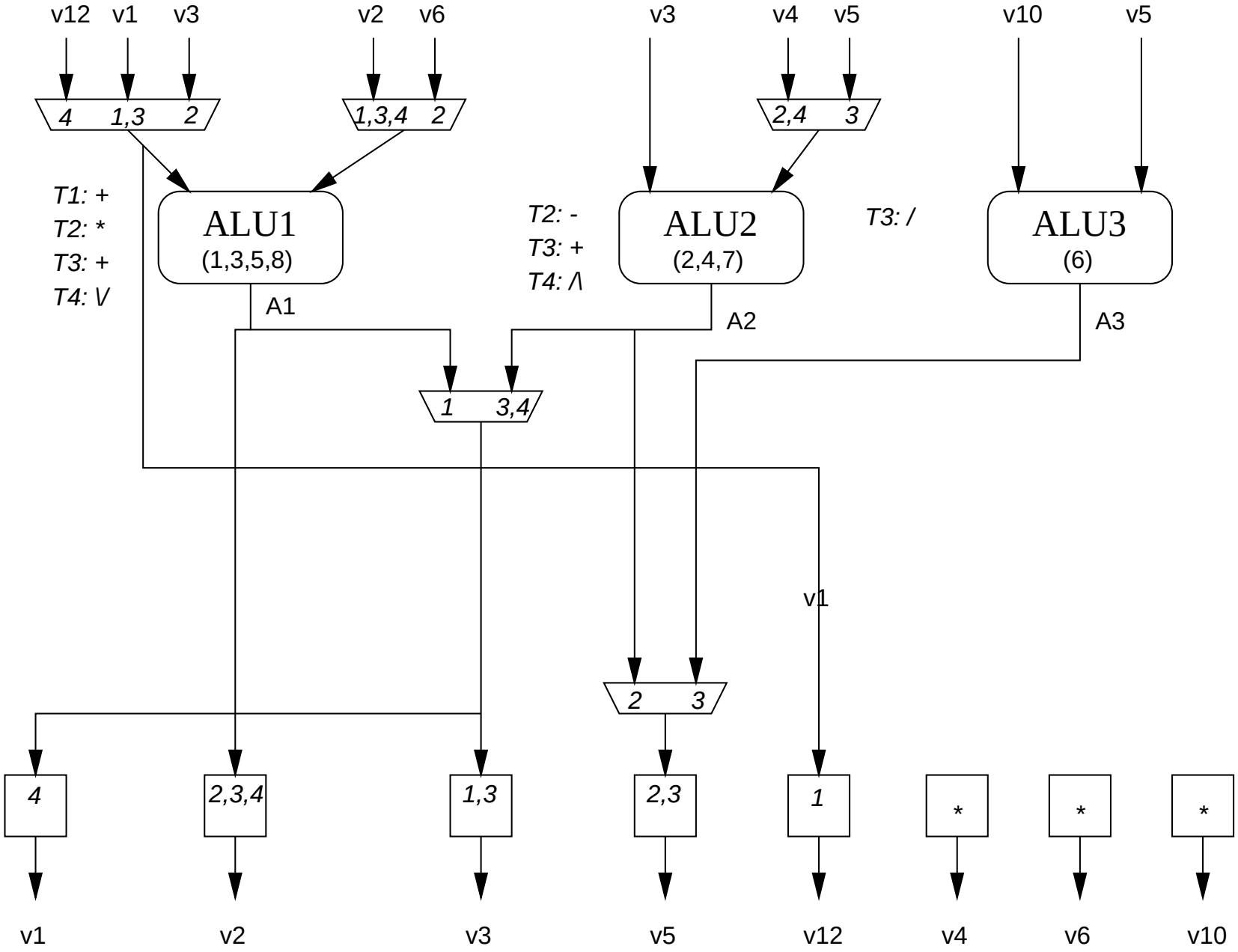
Allocation 6: State 5 deleted; v13 deleted



Allocation 7: Operations allocated to ALU's



Allocation 8: Multiplexers optimized



Allocation 9: Interconnections optimized (?)

Example Behavior

V3 = V1 + V2
V5 = V3 - V4
V7 = V3 * V6
V8 = V3 + V5
V9 = V1 + V7
V11 = V10 / V5
V13 = V3
V12 = V1
V14 = V11 and V8
V15 = V12 or V9
V1 = V14
V2 = V15

Schedule - I

A schedule:

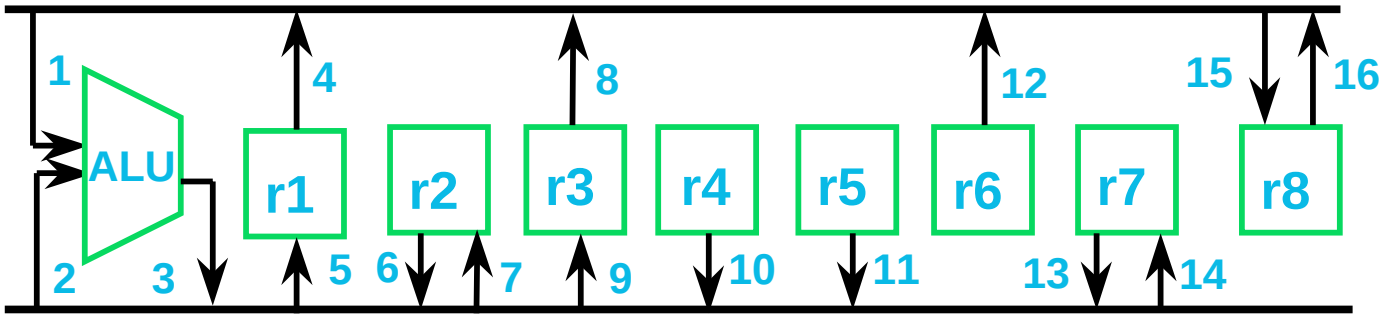
```
r3 = r1 + r2
r7 = r3 - r4
r2 = r3 * r5
r3 = r3 + r7
r2 = r1 + r2
r7 = r6 / r7
r1 = r3 and r7
r2 = r2 or r8
```

```
r8 = r1
```

V1 to V15 merged into r1 to r8

Datapath - I

ALU performs +, -, *, /, and, or



r3 = r1 + r2
r7 = r3 - r4
r2 = r3 * r5
r3 = r3 + r7
r2 = r1 + r2
r7 = r6 / r7
r1 = r3 and r7
r2 = r2 or r8

r8 = r1

Controller - I

Controller:

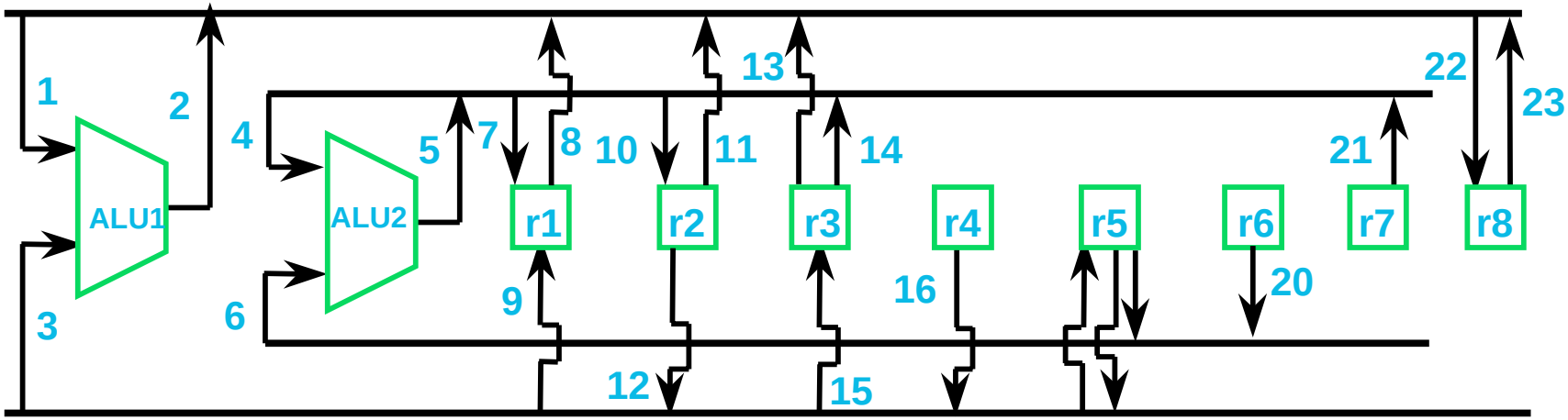
0	S0	S0	N0P	0000000000000000
1	S0	S1	N0P	0000000000000000
-	S1	S2	ADD	1111010010000010
-	S2	S3	SUB	1110000101000100
-	S3	S4	MUL	…
-	S4	S5	ADD	…
-	S5	S6	ADD	
-	S6	S7	DIV	
-	S7	S8	AND	
-	S8	S0	OR	…

Schedule and Datapath - II

r3 = r1 + r2
r5 = r3 - r4
r3 = r3 + r5
r2 = r1 and r2
r2 = r8 + r2

r8 = r1

r2 = r3 * r6
r5 = r5 * r7
r1 = r3 or r5



Controller - II

Controller

0	S0	S0	NOP	NOP	00000000000000000000000
1	S0	S1	NOP	NOP	00000000000000000000000
-	S1	S2	ADD	NOP	11100001000100100000010
-	S2	S3	SUB	MUL	…
-	S3	S4	ADD	DIV	…
-	S4	S5	AND	OR	
-	S5	S6	ADD	NOP	…