Lecture 18

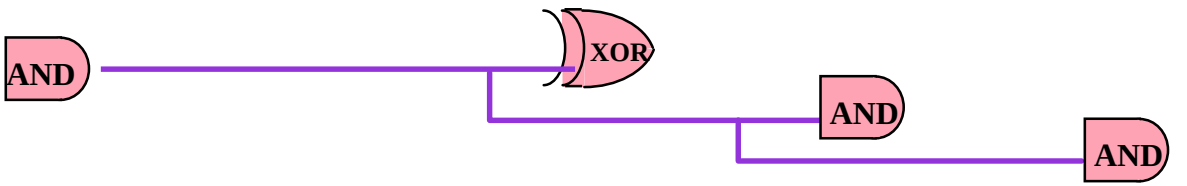
BUS and MEMORY

Slides of Adam Postula used

SIGNAL PROPAGATION

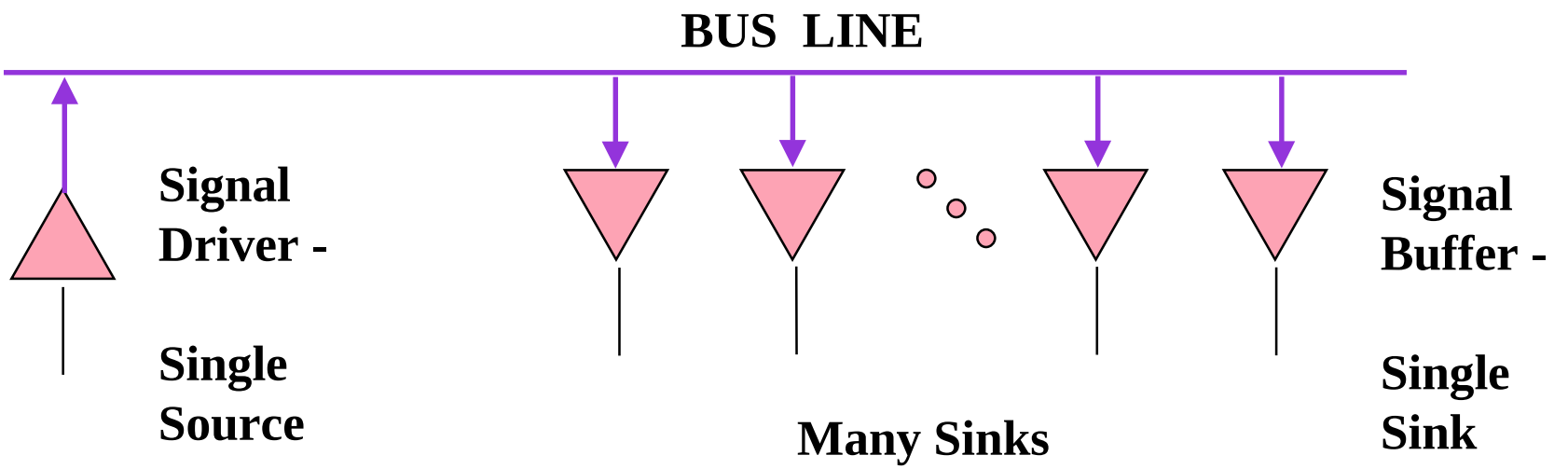
FROM ONE SOURCE TO MANY SINKS

A



Signal line - FANOUT = 3

B



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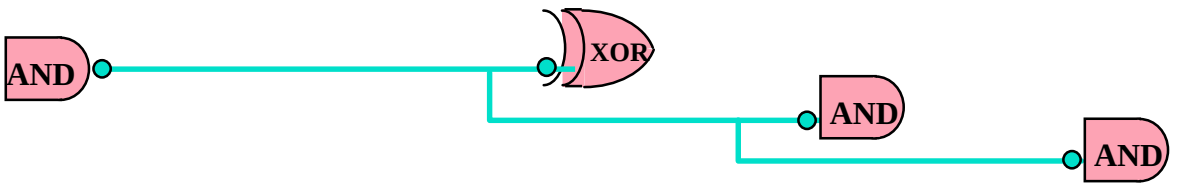
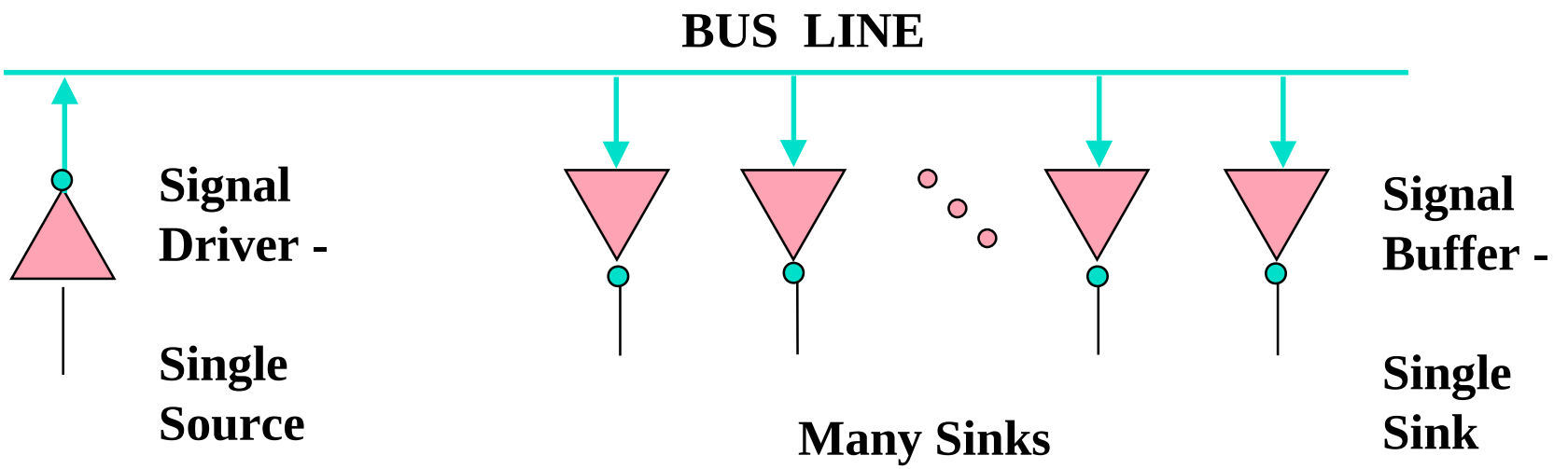


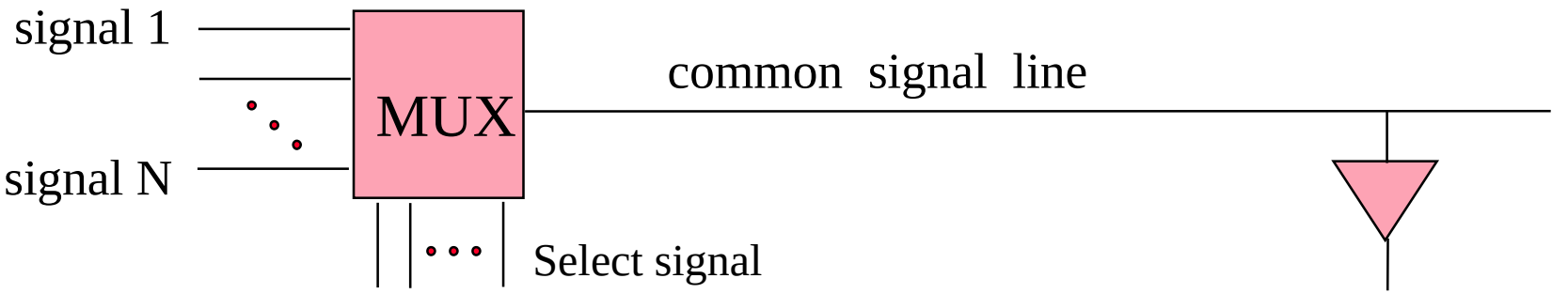
Signal line - FANOUT = 3

B



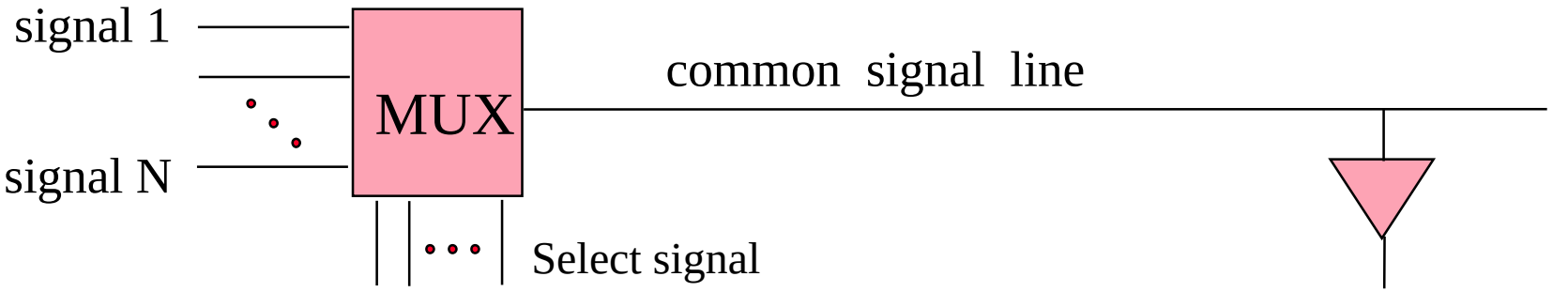
SIGNAL PROPAGATION

FROM MANY SOURCES TO ONE SINK

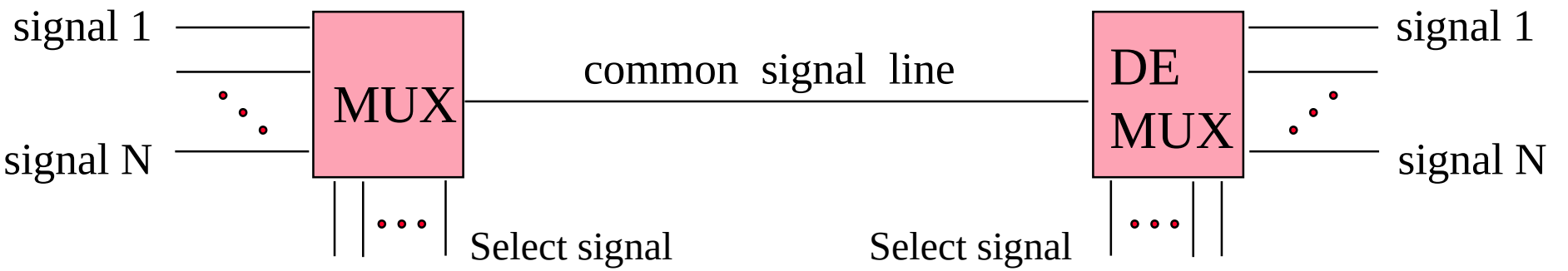


SIGNAL PROPAGATION

FROM MANY SOURCES TO ONE SINK

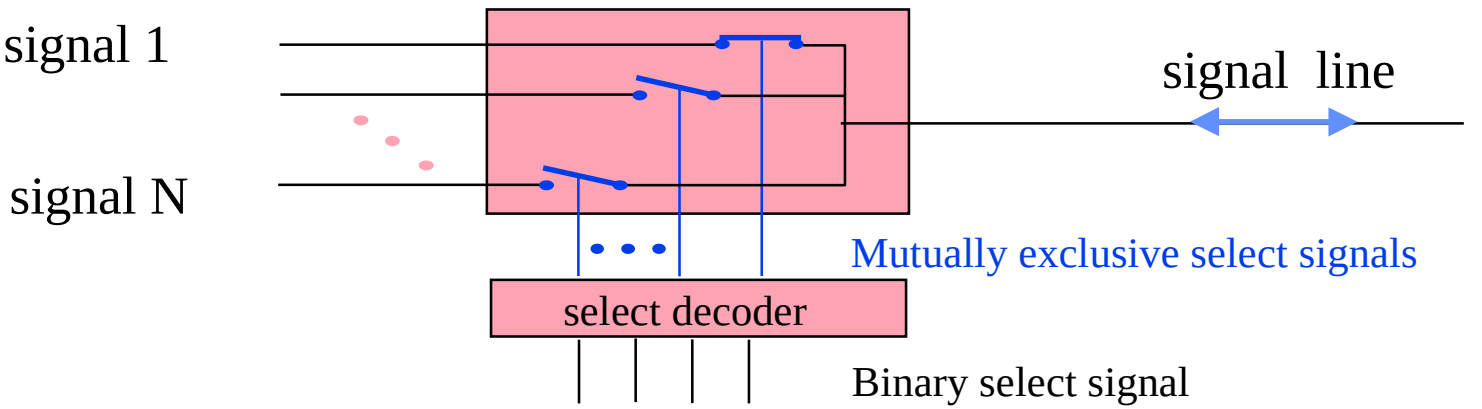


FROM MANY SOURCES TO MANY SINKS



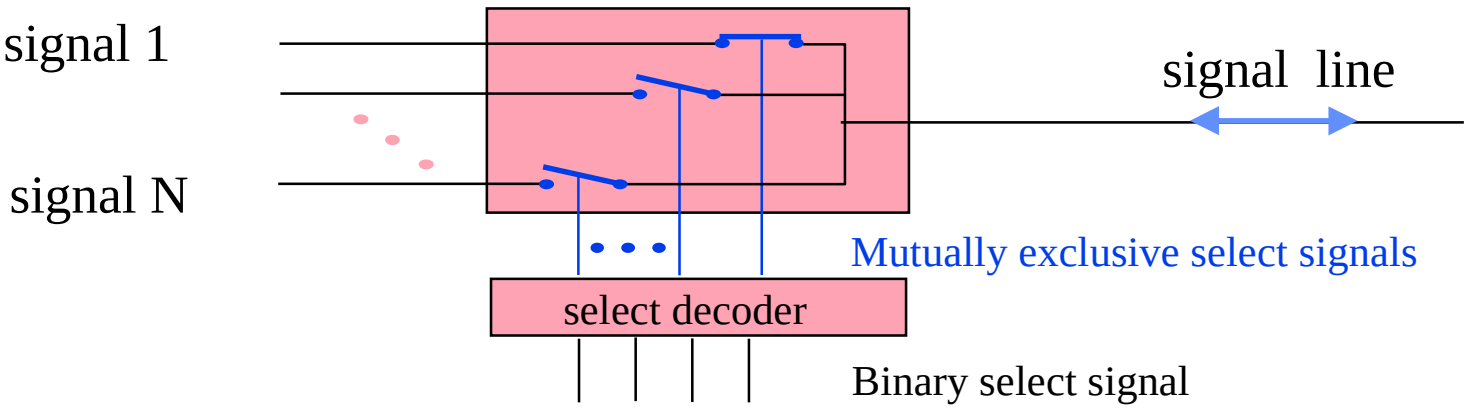
TriState Buffer Concept

Switch model of a multiplexer

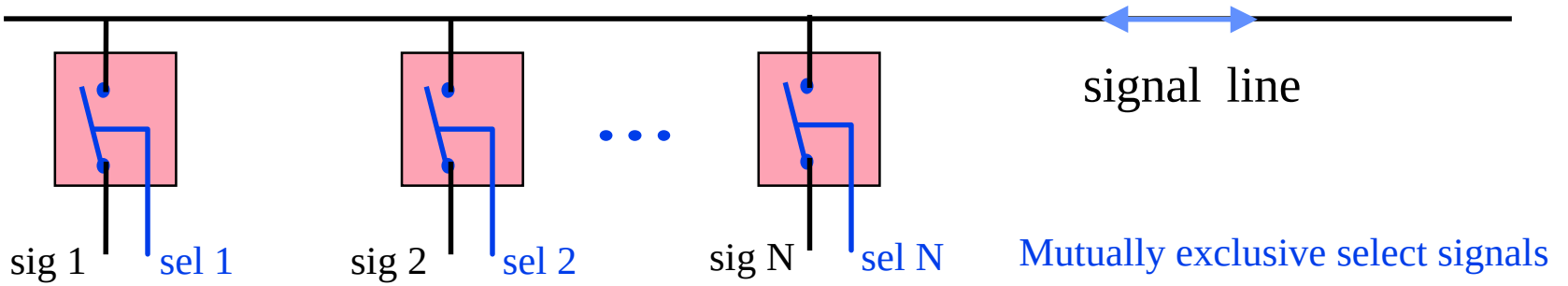


TriState Buffer Concept

Switch model of a multiplexer

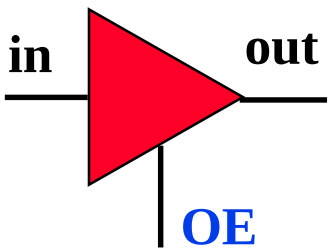


TRISTATE buffer signal drivers - a DISTRIBUTED MULTIPLEXER

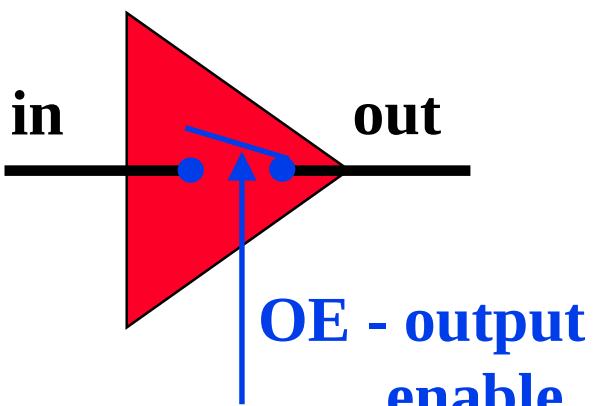


TriState Buffer

SYMBOLS



SWITCH MODEL

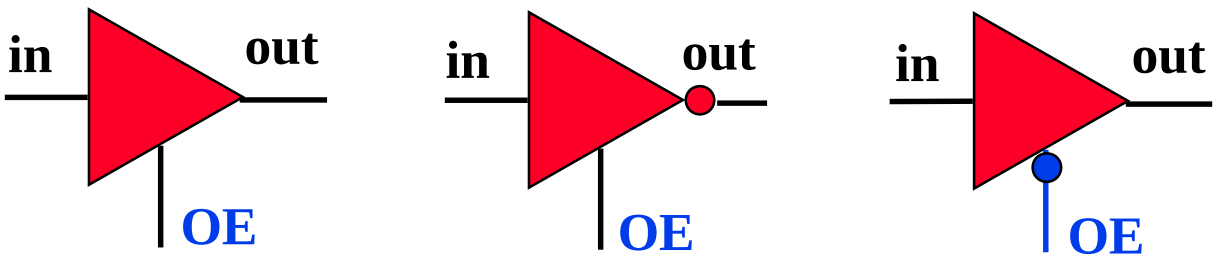


OE	in	out
0	0	Z
0	1	Z
1	0	0
1	1	1

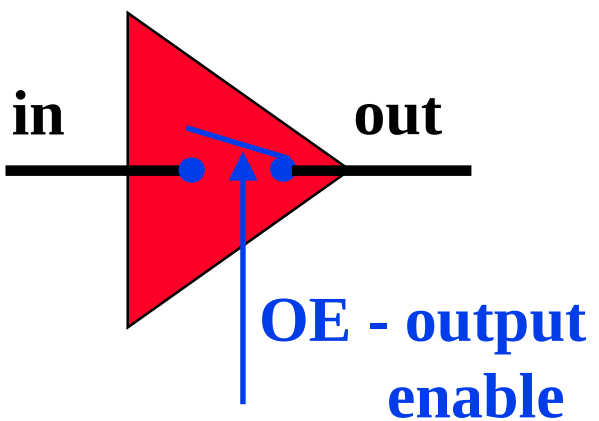
Z = High Impedance output not connected to input

TriState Buffer

SYMBOLS

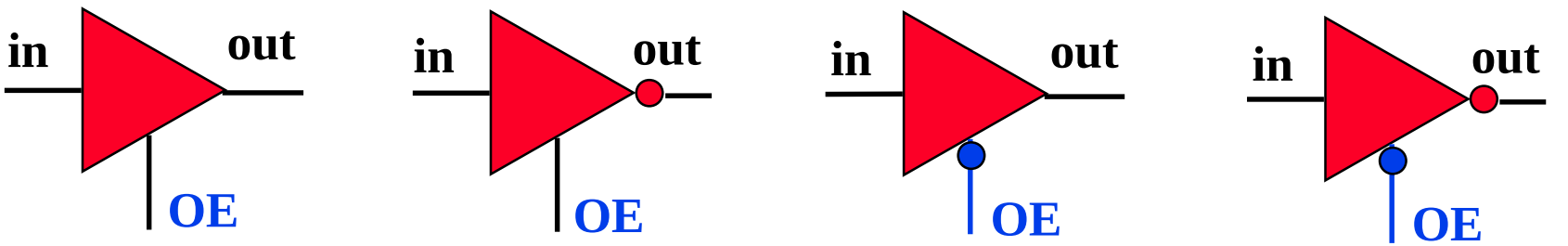


SWITCH MODEL

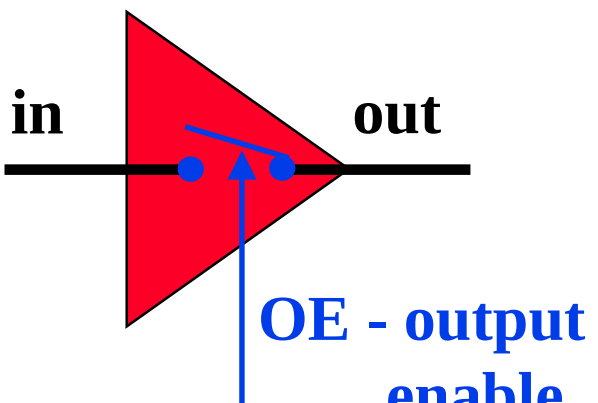


TriState Buffer

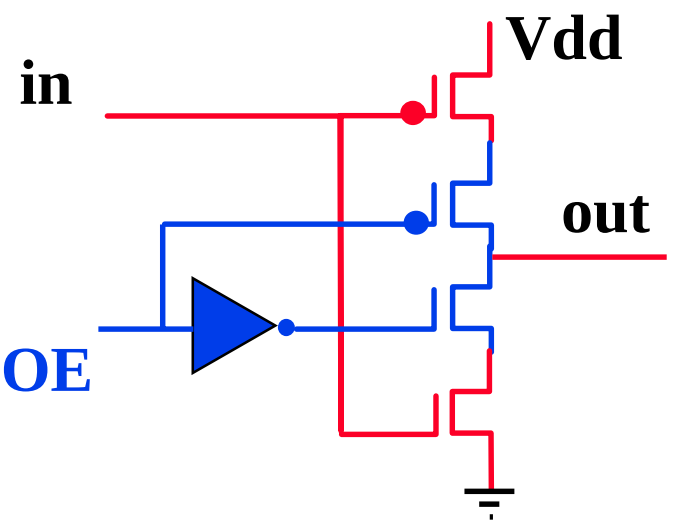
SYMBOLS



SWITCH MODEL

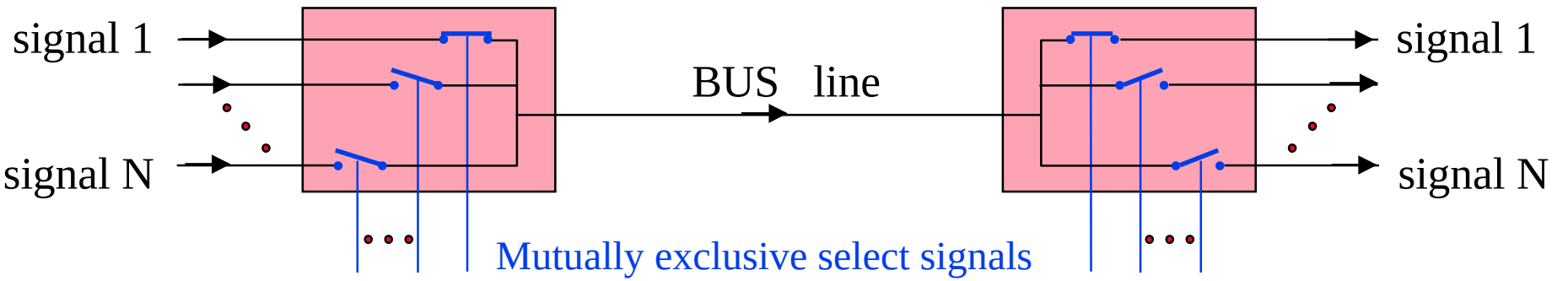


CMOS IMPLEMENTATION



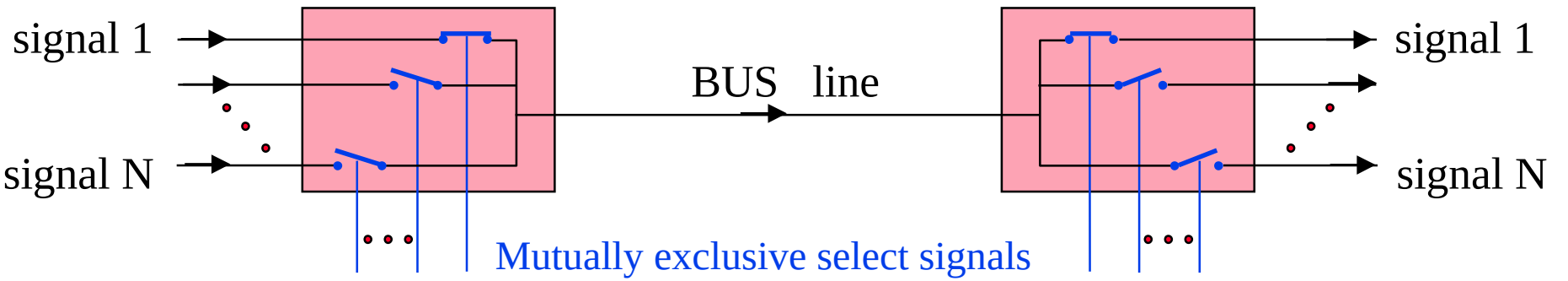
UNIDIRECTIONAL BUS LINE

Propagation from many sources to many sinks

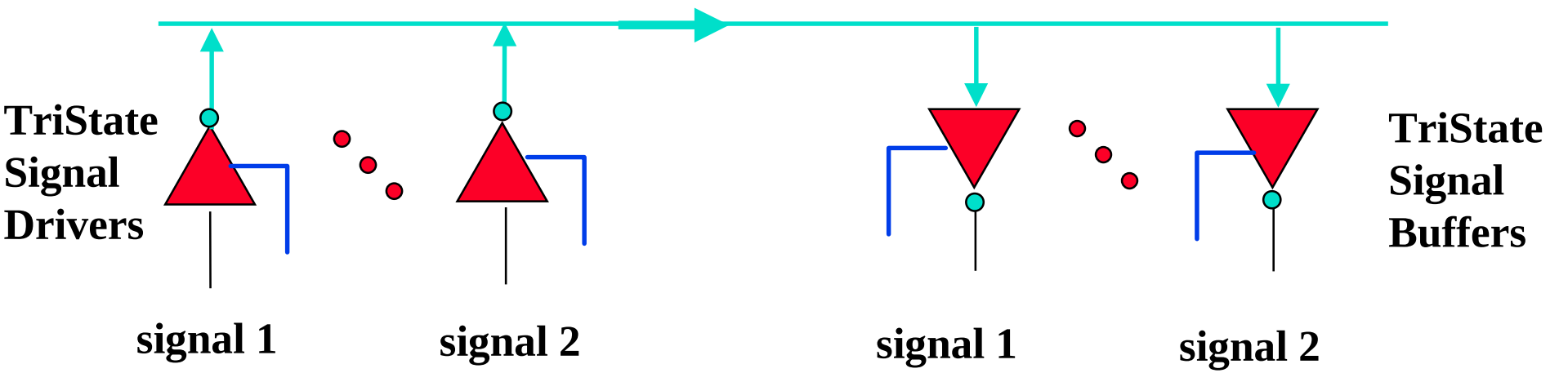


UNIDIRECTIONAL BUS LINE

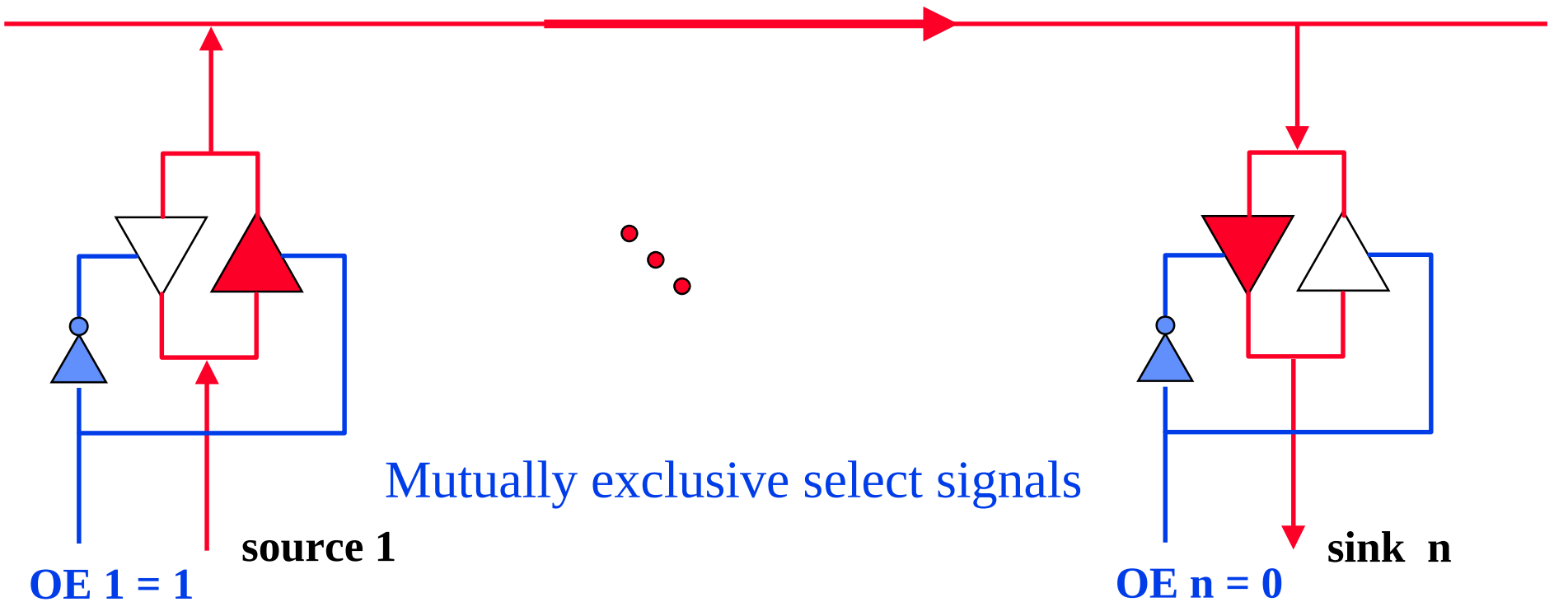
Propagation from many sources to many sinks



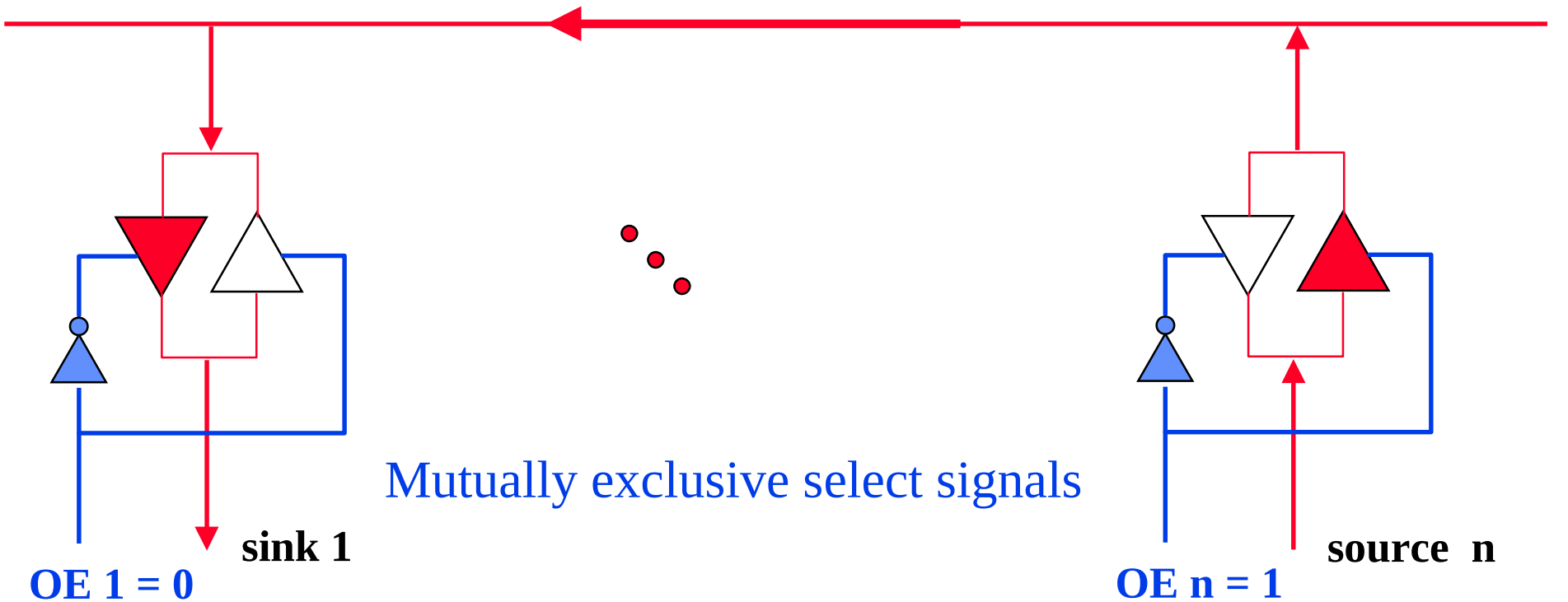
UNIDIRECTIONAL BUS LINE



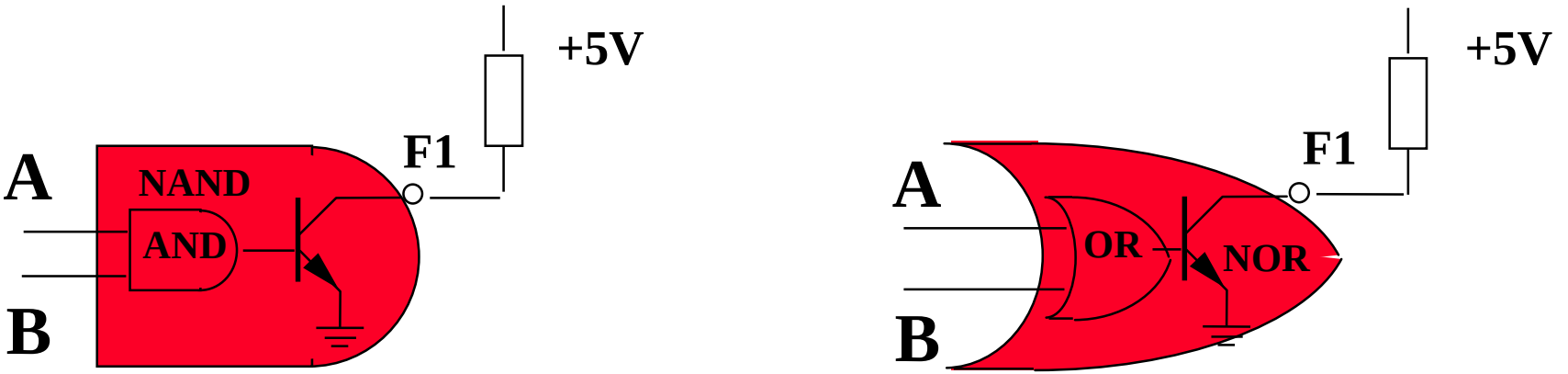
BIDIRECTIONAL BUS LINE



BIDIRECTIONAL BUS LINE



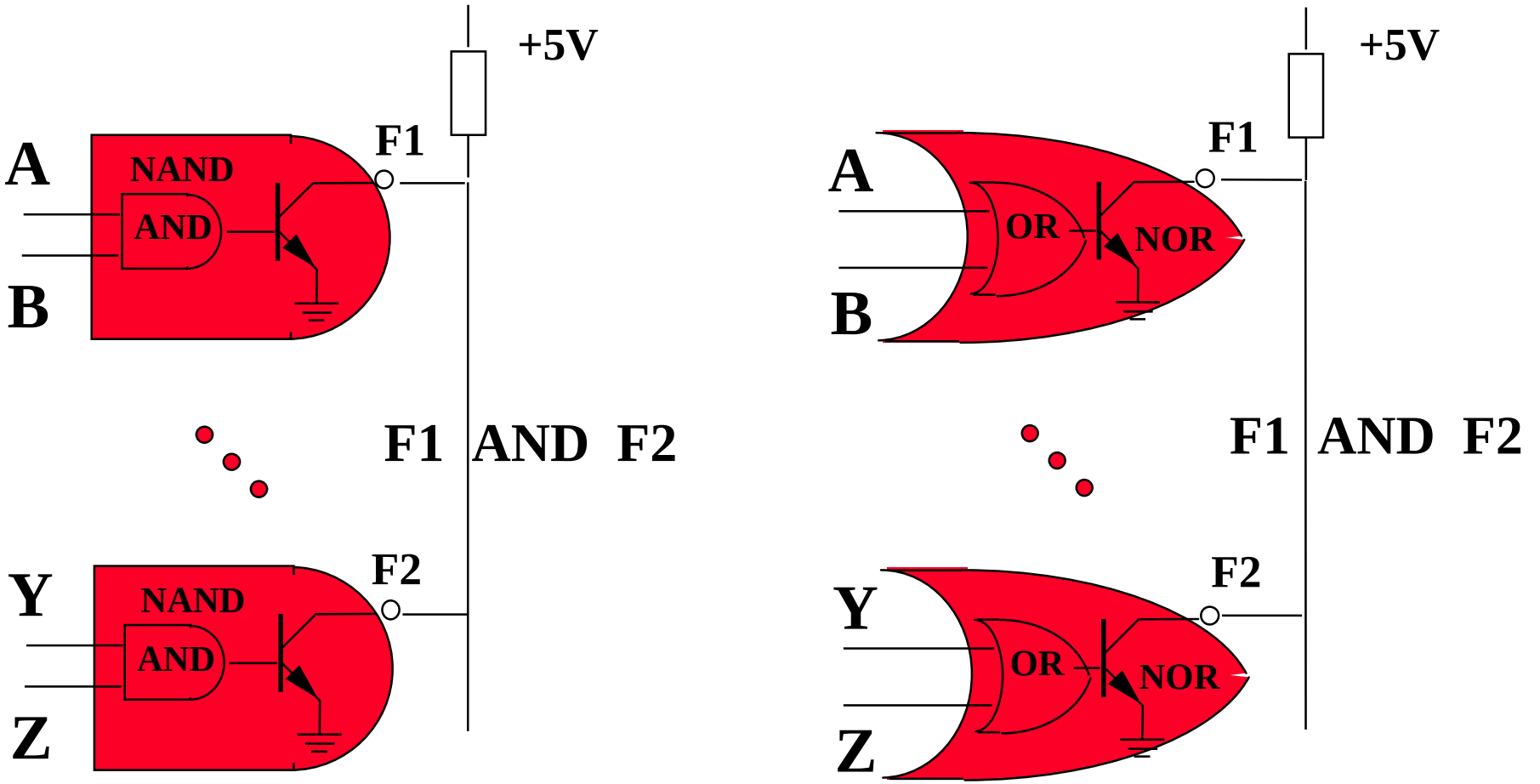
WIRED LOGIC



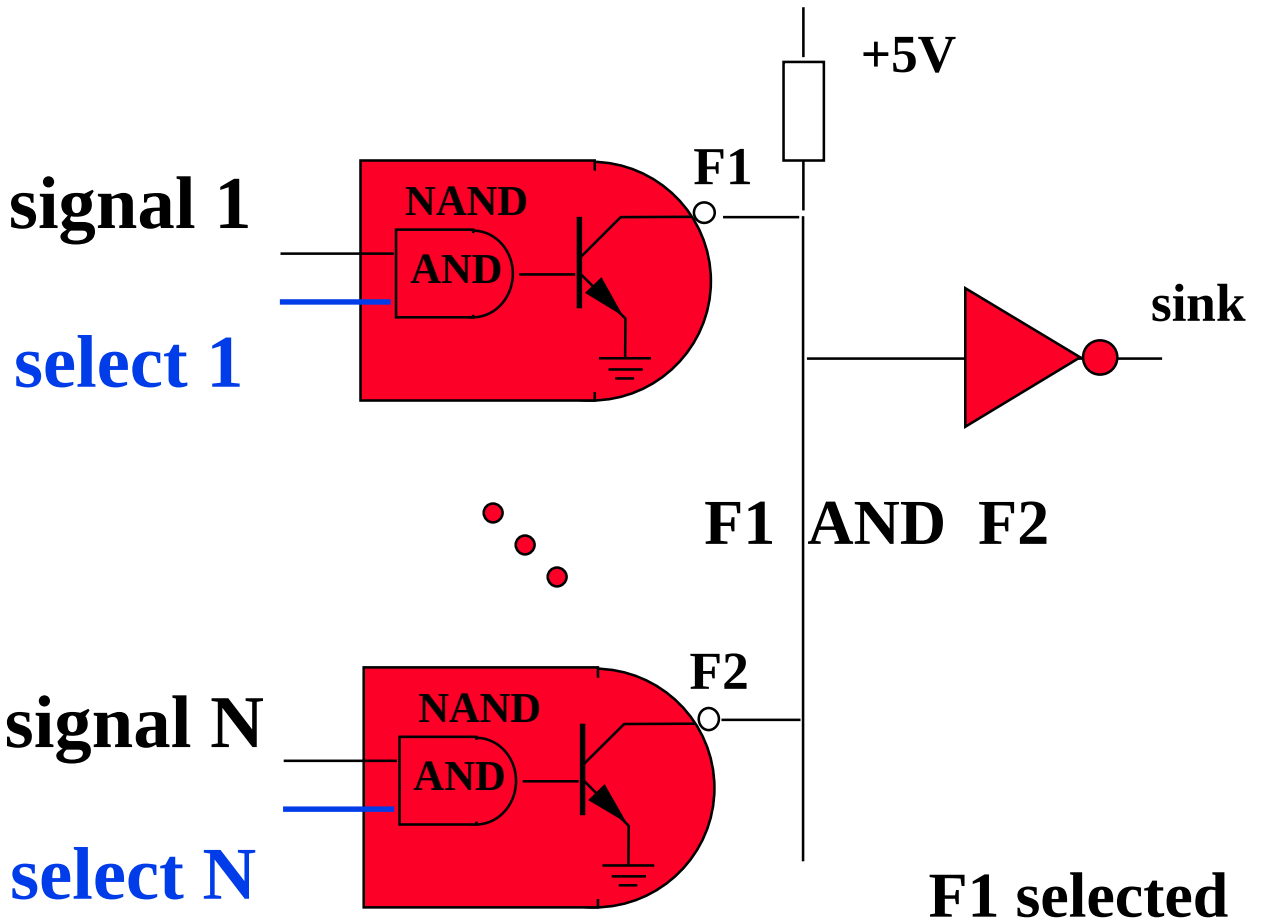
TRANSISTORS WORK AS INVERTERS

OPEN COLLECTORS NEED PULL_UP RESISTORS

WIRED LOGIC

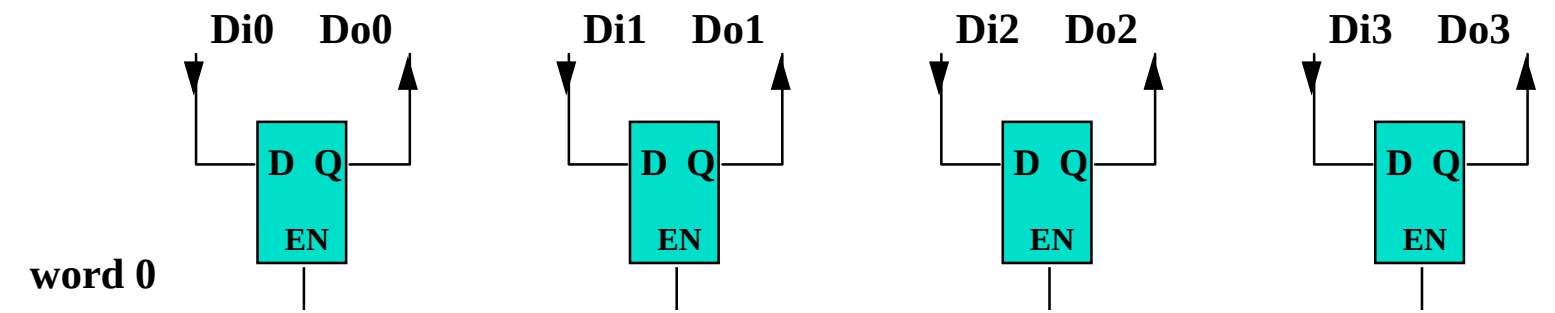

+5V
A
B
NAND
AND
F1
F1 AND F2
Y
Z
NAND
AND
F2
+5V
A
B
OR
NOR
F1
F1 AND F2
Y
Z
OR
NOR
F2

WIRED LOGIC BUS

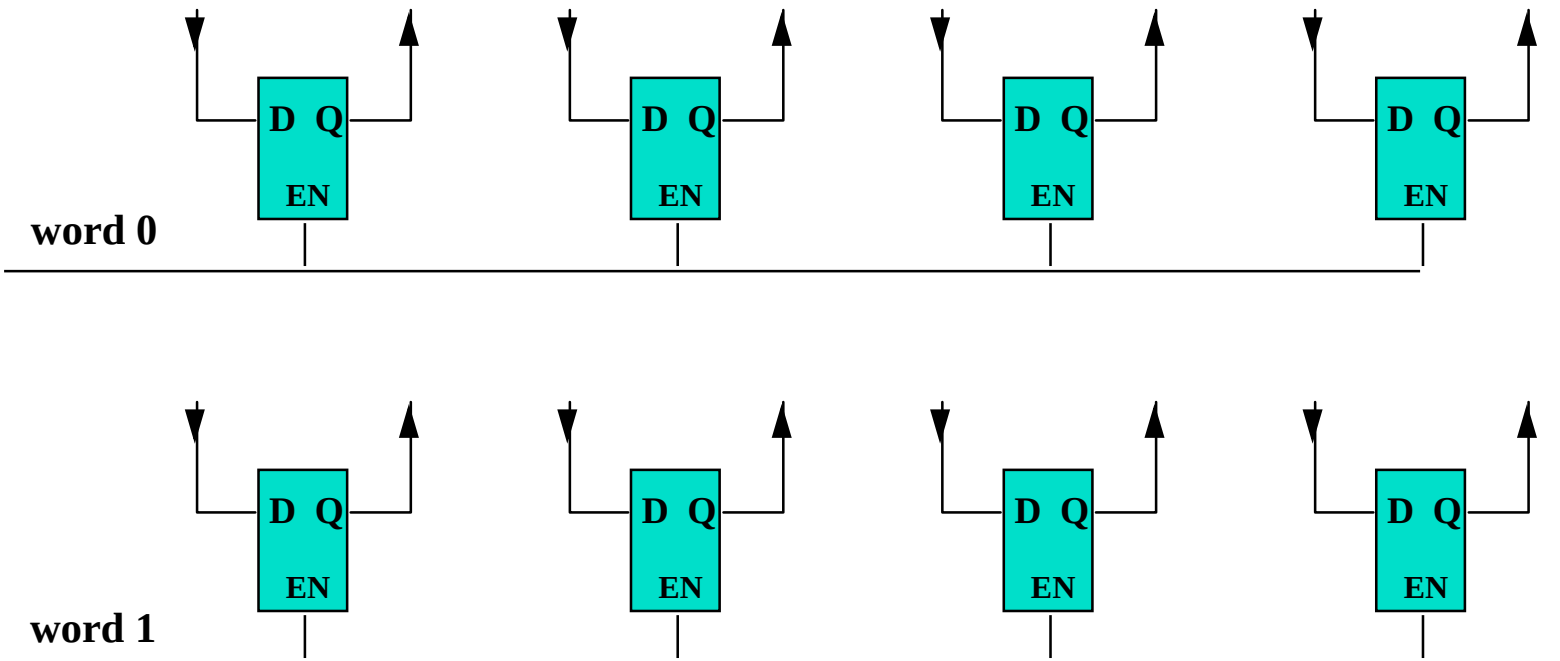


sel1	sig1	F1
0	0	1
0	1	1
1	0	1
1	1	0

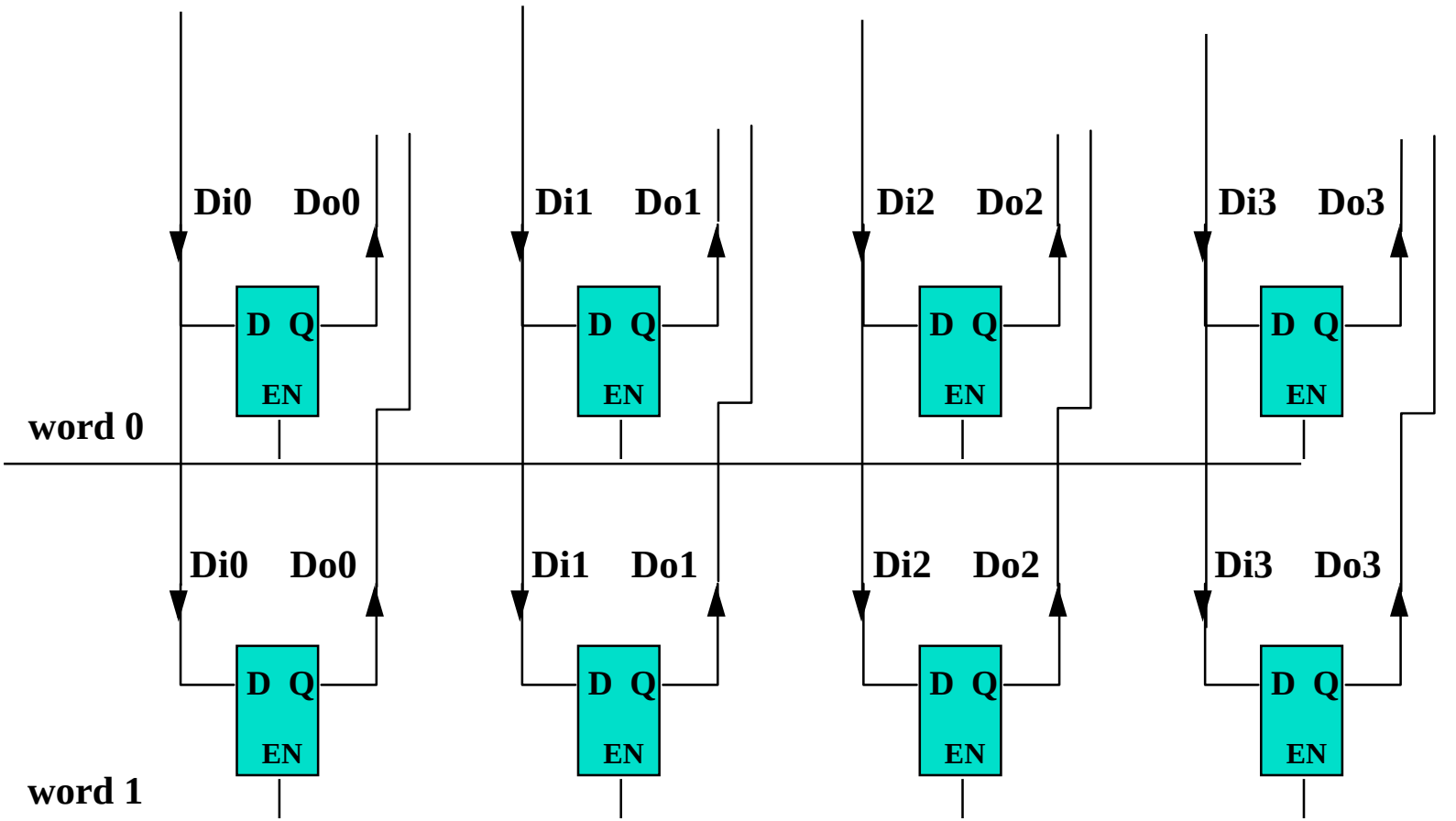
REGISTER FILE



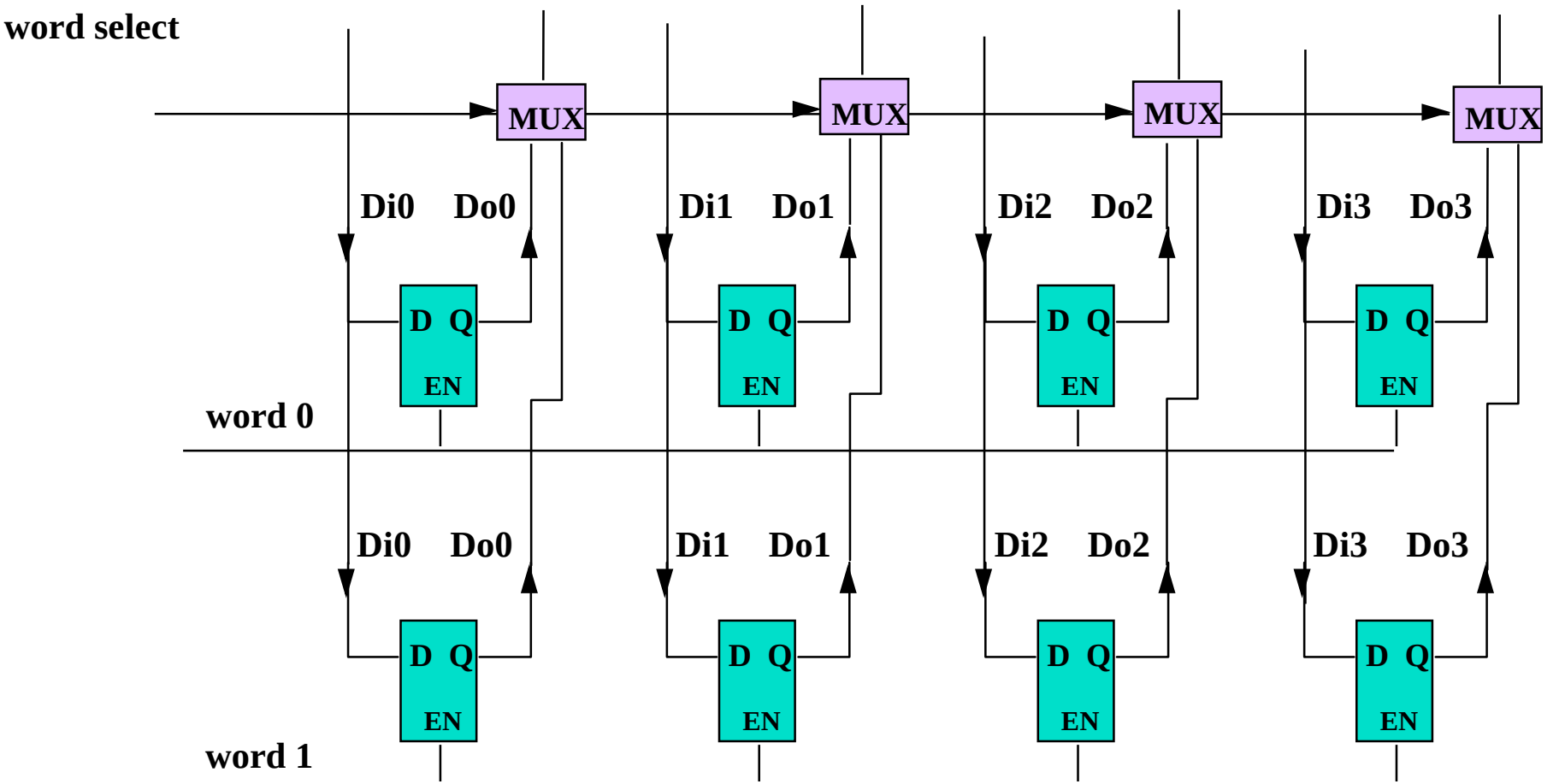
REGISTER FILE



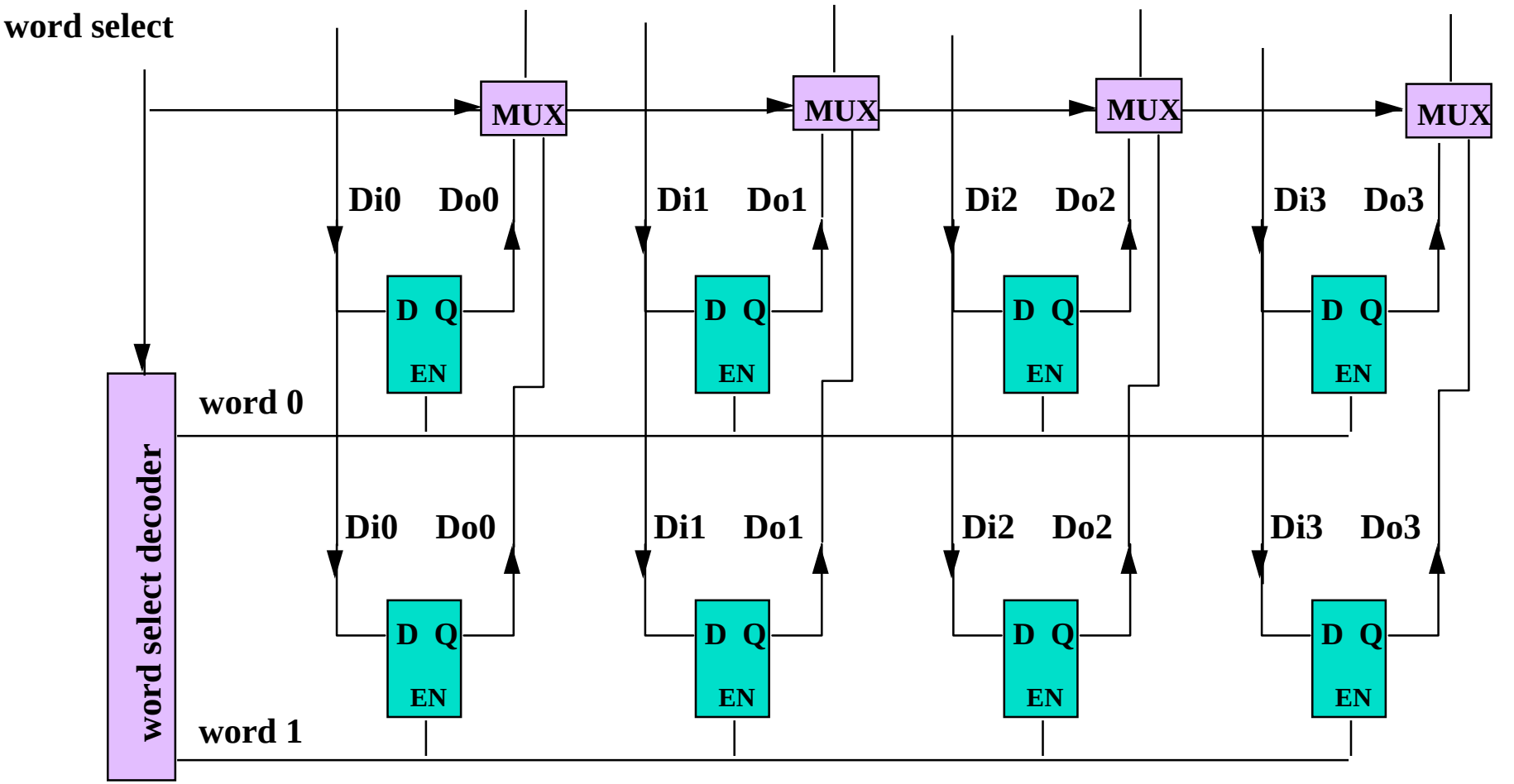
REGISTER FILE



REGISTER FILE

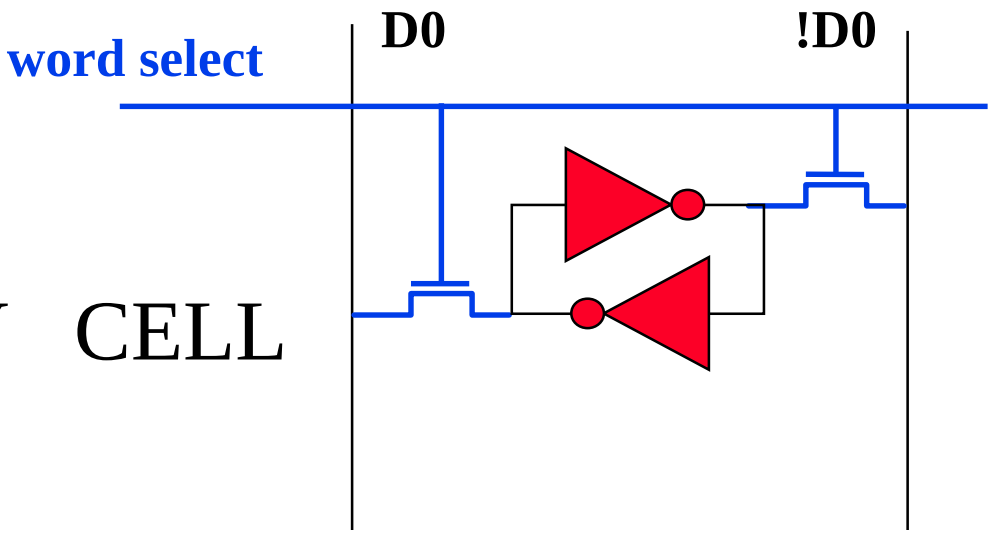


REGISTER FILE



MEMORY ELEMENTS

STATIC
MEMORY CELL

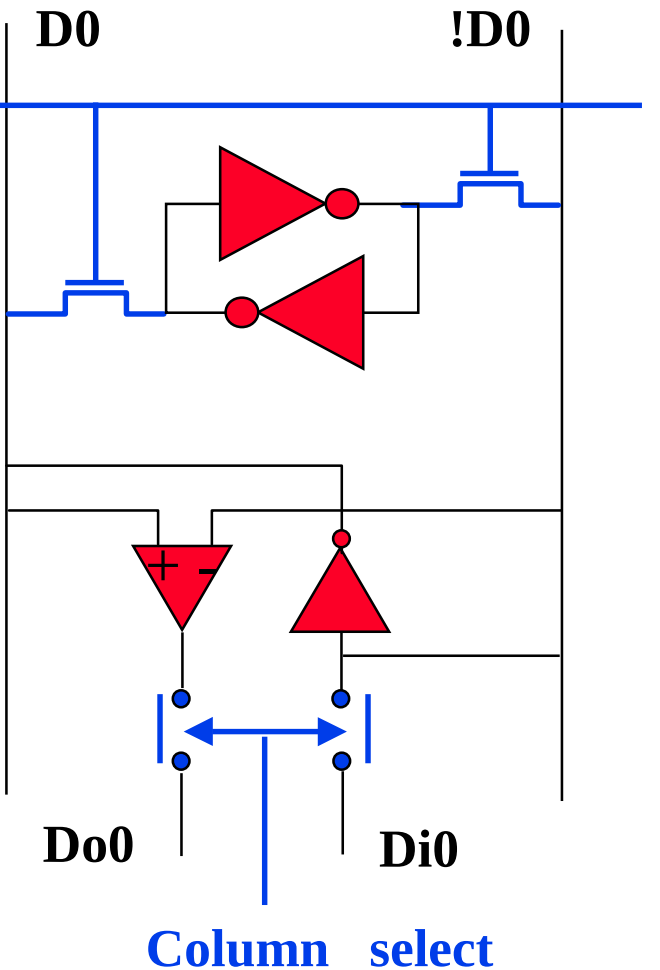


THE BASIC ELEMENT IS A STATIC LATCH THAT HOLDS THE STORED VALUE AS LONG THE POWER IS ON.

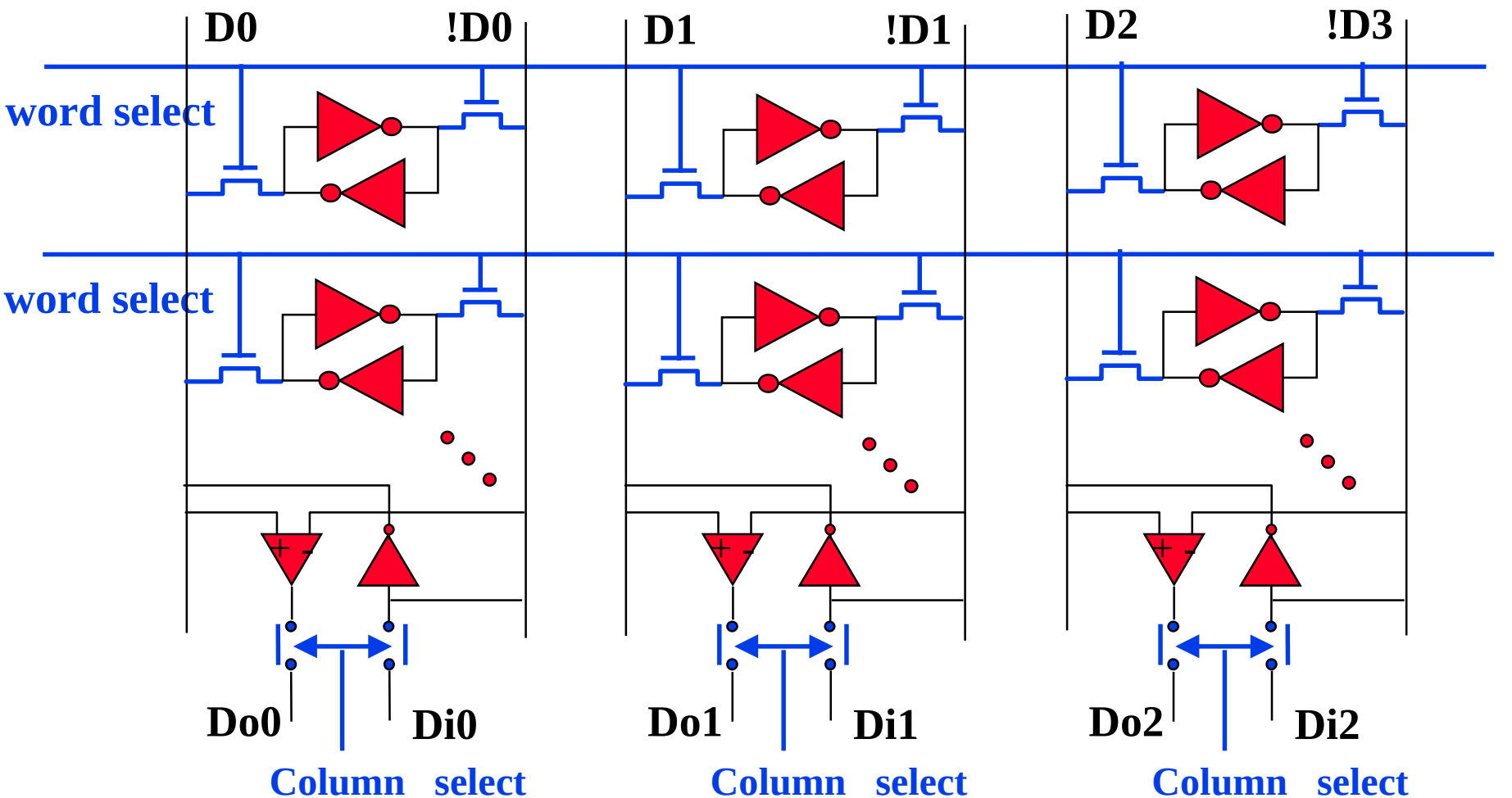
MEMORY ELEMENTS

STATIC MEMORY CELL

READ WRITE CIRCUITRY
(conceptual view)



MEMORY ARRAY



RAM - Random Access Memory

- Each word in the RAM memory can be read by giving its address and observing the data lines after some time.
- Each word can be re-written by giving its address, presenting the new data and keeping it stable for some time.
- Addressing can be random (there are no requirements for any sequence in addresses) - hence Random Access Memory.
- Storage matrix is usually very large and organized as a square matrix of word cells.

What have we learnt?

- TriState buffers allow to connect many signal sources
  to the same signal line. Wired logic can provide the same functionality although is less popular.
- Flip-flops can be organized in registers, registers in register files.
- RAM - Random Access Memory allows to read/write data at a randomly chosen address.