TOPICS FOR MIDTERM EXAM

Marek Perkowski

1. Boolean Algebra, DeMorgan's Laws. EXOR laws.
2. Unate Set Covering Problem.
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4. Maximum cliques
5. Compatibility and Incompatibility graphs and their uses
6. Partitioning to cliques
7. Covering with cliques
8. Graph coloring. Chromatic number. Perfect graphs.
9. Shortest and longest path in a graph.
10. Using Karnaugh Maps to minimize Sum of Product expressions
11. Using Karnaugh Maps to minimize Product of Sums and Exclusive-Or Sum of Product expressions
12. Calculate cofactors and vacuous cofactors using Kmaps, DDs, and expressions.
13. Boolean Difference of a completely and incompletely specified Boolean function
14. Shannon, Positive Davio and Negative Davio expansions.
15. Binary Decision Diagrams
16. Use of Binary Decision Diagrams to create a network from multiplexers.
17. Kronecker Functional Decision Diagrams, Functional (positive Polarity) Decision Diagrams, Reed-Muller Diagrams and Pseudo-Kronecker Functional Decision Diagrams.
18. The concept of canonical representation. Examples of canonical and non-canonical representations.
19. Algebraic methods of circuit synthesis – various factorization rules.
20. Graphical inhibition methods for logic synthesis.
21. Role of multiplexers in data path design
22. Technology mapping from generic netlists.
23. Canonical AND/EXOR forms: Positive Polarity Reed-Muller, Fixed Polarity Reed-Muller, Generalized Reed-Muller and S/D Trees and Forms
24. Stuck-at-one and stuck-at-zero faults. Delay faults.
25. The concept of test for combinational and sequential circuits.
26. Examples of naïve test generation for given fault.
27. Using set covering to minimize the set of tests for a given set of faults.

28. Test equivalence and compression
29. Use of PPRM and FPRM to design highly testable circuits.
30. Synthesis of three-level circuits and TANT circuits.
31. Vacuous variables of an incompletely specified functions. Finding their all sets.
32. Recursive Tree Paradigm applications: finding prime implicants, solving covering problem, etc.
33. Boolean equations and Petrick functions.
34. Satisfiability and generalized satisfiability problems.
35. Reduction of AND/OR graphs search to satisfiability.
36. Complementation, satisfiability and tautology – mutual relations. Ways of calculating and checking them.
37. Pareto optimization in technology mapping.
38. Pipelined circuits and their control
39. Finite State Machine for a data path. Simple non-optimized examples.
40. Shift registers and counters. Optimization of logic part.
41. Symmetric functions of various polarities. Finding symmetric subsets and test for total symmetry of a function using Kmap.
42. Lattice Diagrams with Shannon nodes, Davio Nodes, mixed nodes.
43. Generalizations of Lattice diagrams. Regular structures for layout and logic.
44. Layout Driven logic synthesis
45. Field Programmable Gate Arrays (FPGAs) – design issues and applications.
46. Programmable Logic Arrays.
47. Physical design algorithm fundamentals: floorplanning and placement, routing, partitioning.
48. The concept of multiple-valued logic.
49. Galois addition and Galois multiplication, sum-modulo-k and Latin Square gates. Their use in Linearly Independent expansions for circuit design.
50. The concept of functional decomposition
51. Comprehensive Design Automation systems. Design issues.
52. The concept of quantum logic. Examples of quantum gates.
53. Analysis of a quantum circuit. Unitary matrices, matrix multiplication and Kronecker (tensor) product.
54. Reversible logic and gates. Examples.
55. Designing a very simple circuit using arbitrary reversible gates, Fredkin, Toffoli, Feynman, inverter.

56. You should be able to convert any representation to any other representation, for instance among netlist of gates, set of expressions, Karnaugh Maps, Binary Decision Diagrams, Lattices, network of multiplexers, etc.