Lecture 19

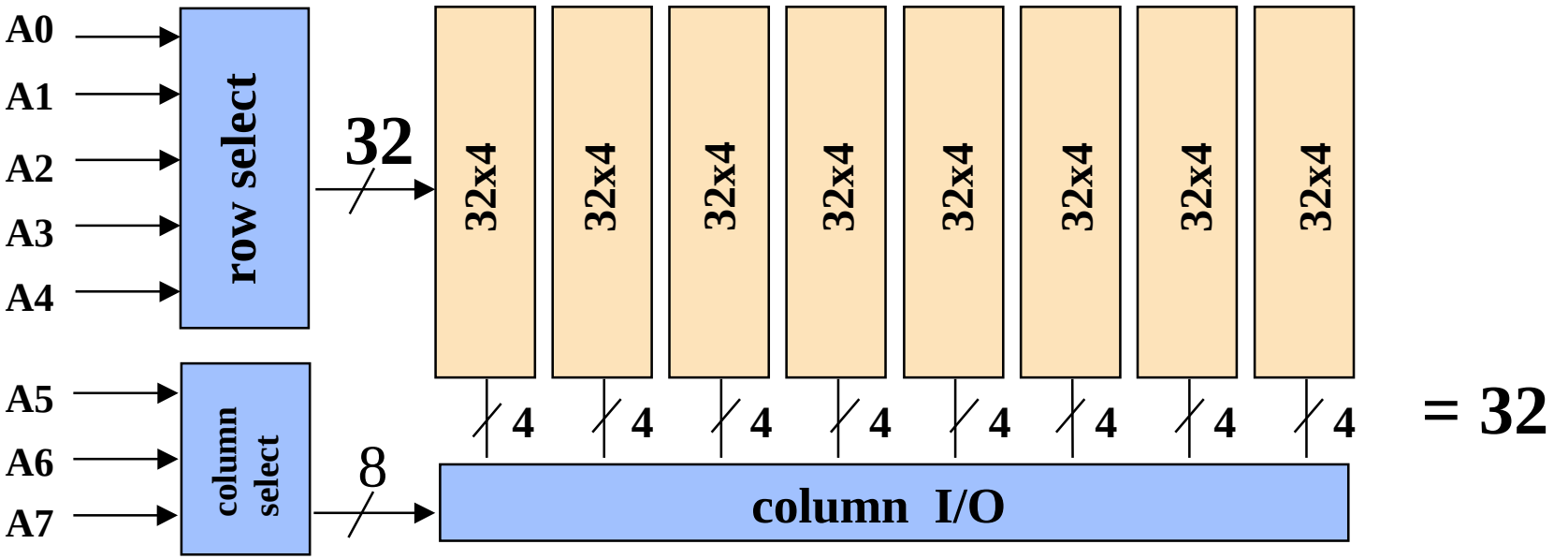
MEMORY
RAM,ROM and memory systems

Slides of Adam Postula used

RAM - Random Access Memory

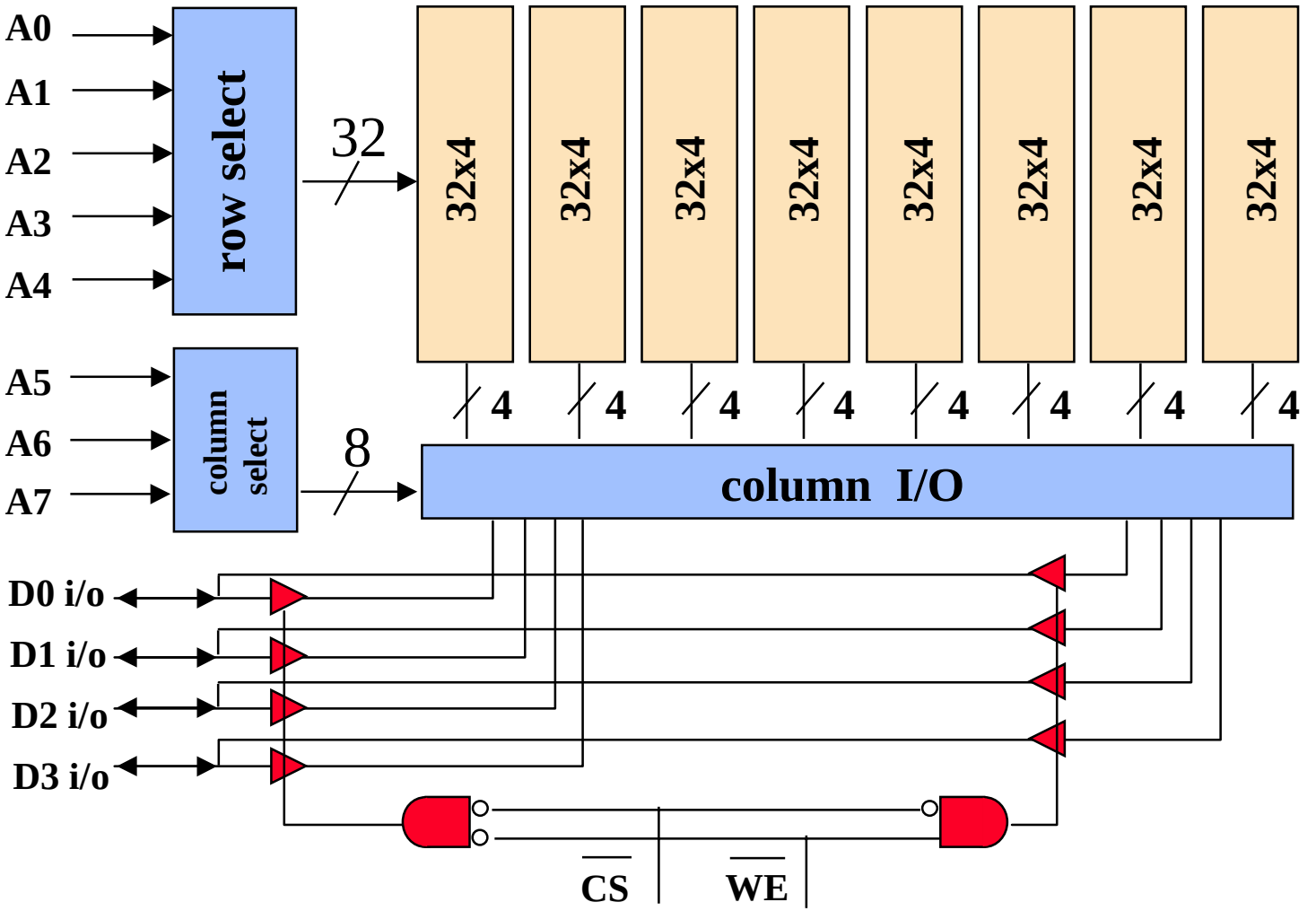
- Each word in the RAM memory can be read by giving its address and observing the data lines after some time.
- Each word can be re-written by giving its address, presenting the new data and keeping it stable for some time.
- Addressing can be random (there are no requirements for any sequence in addresses) - hence Random Access Memory.
- Storage matrix is usually very large and organised as a square matrix of word cells.

256x4 bit RAM internal organisation

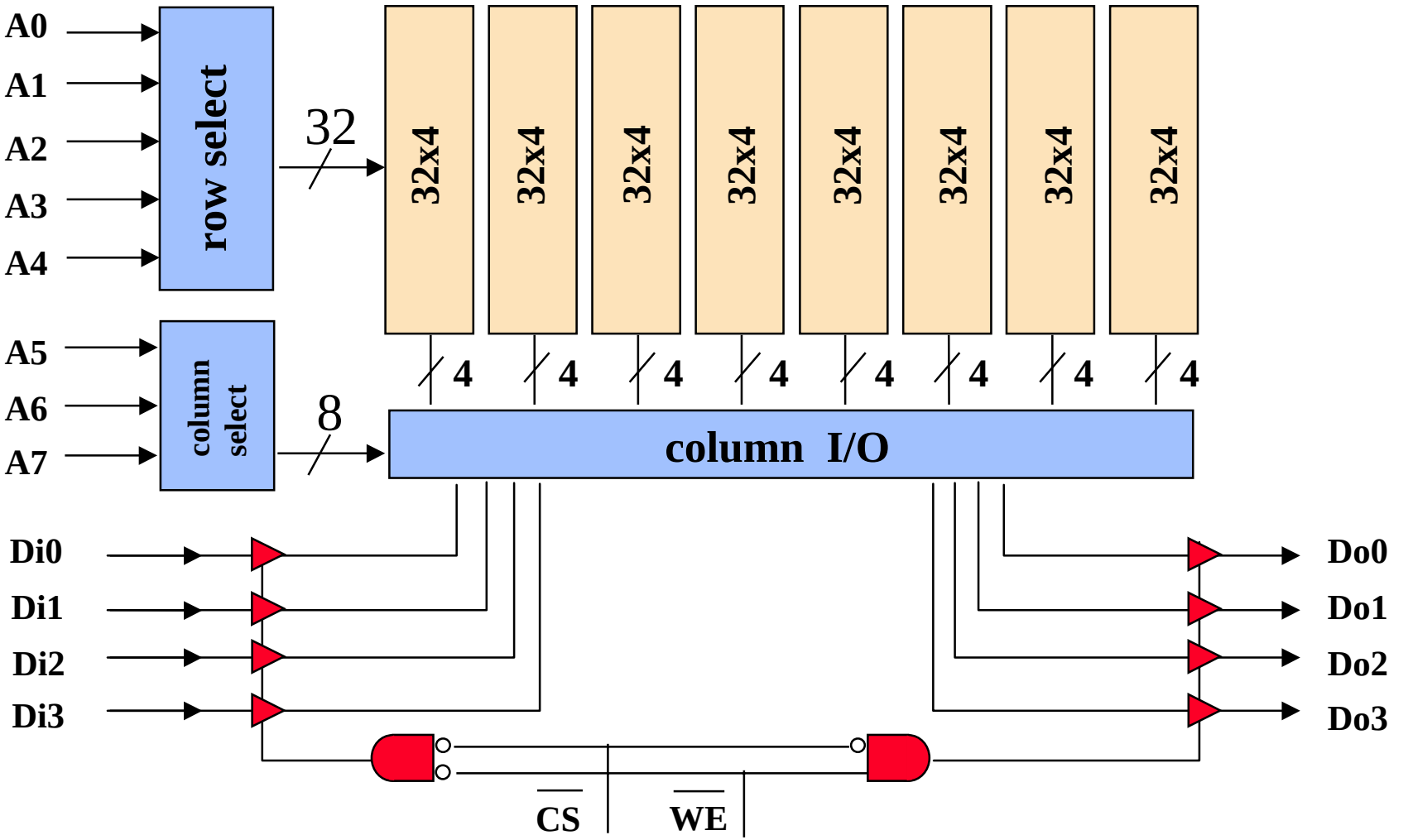


A square storage matrix (32 x 32) makes an optimal design for the layout and delay minimisation.

256x4 bit RAM
Common I/O data lines

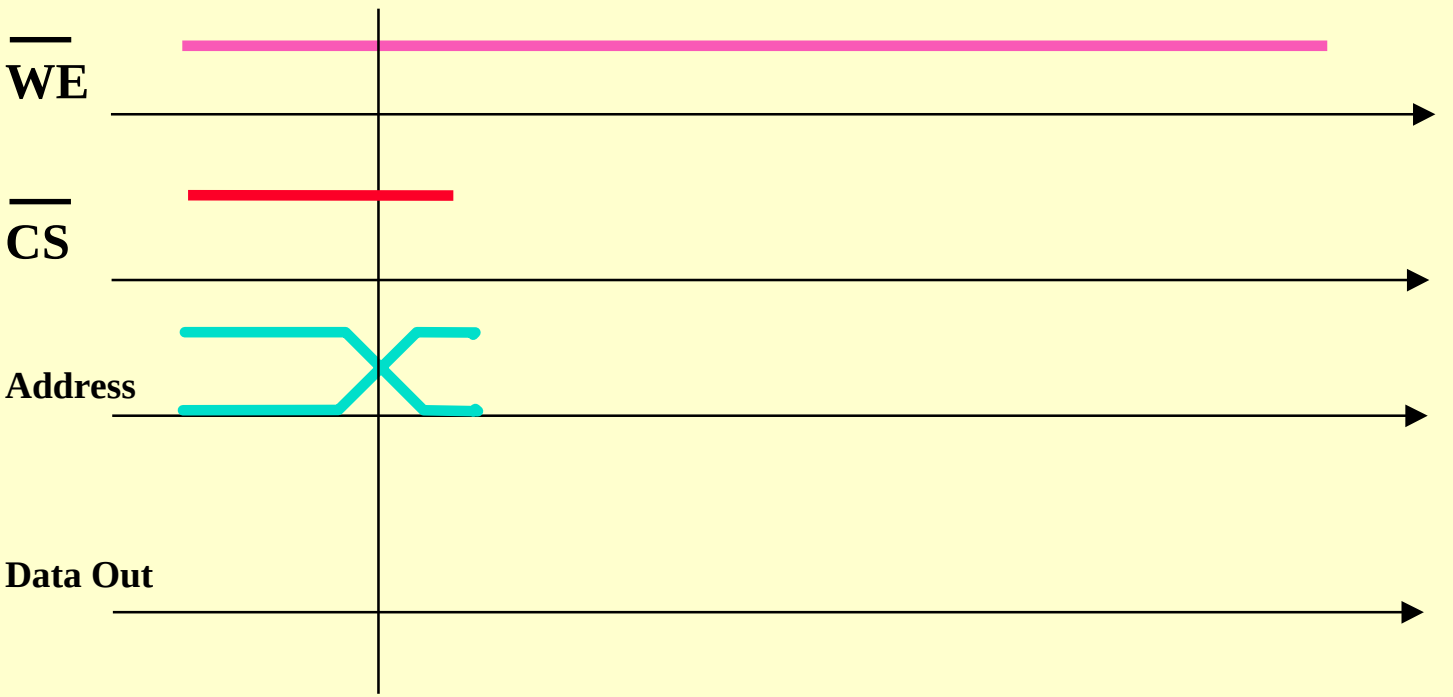


256x4 bit RAM
Separate I/O data lines



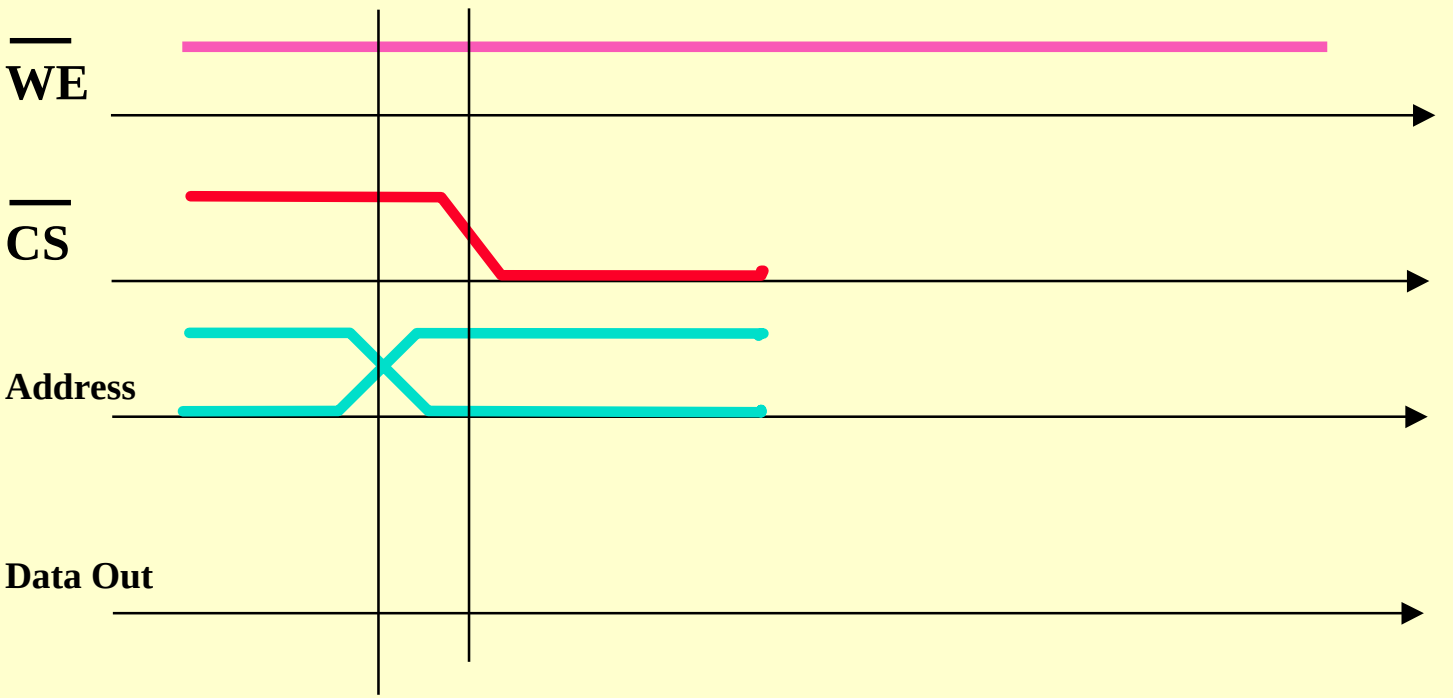
Read RAM Timing

- **READ CYCLE**



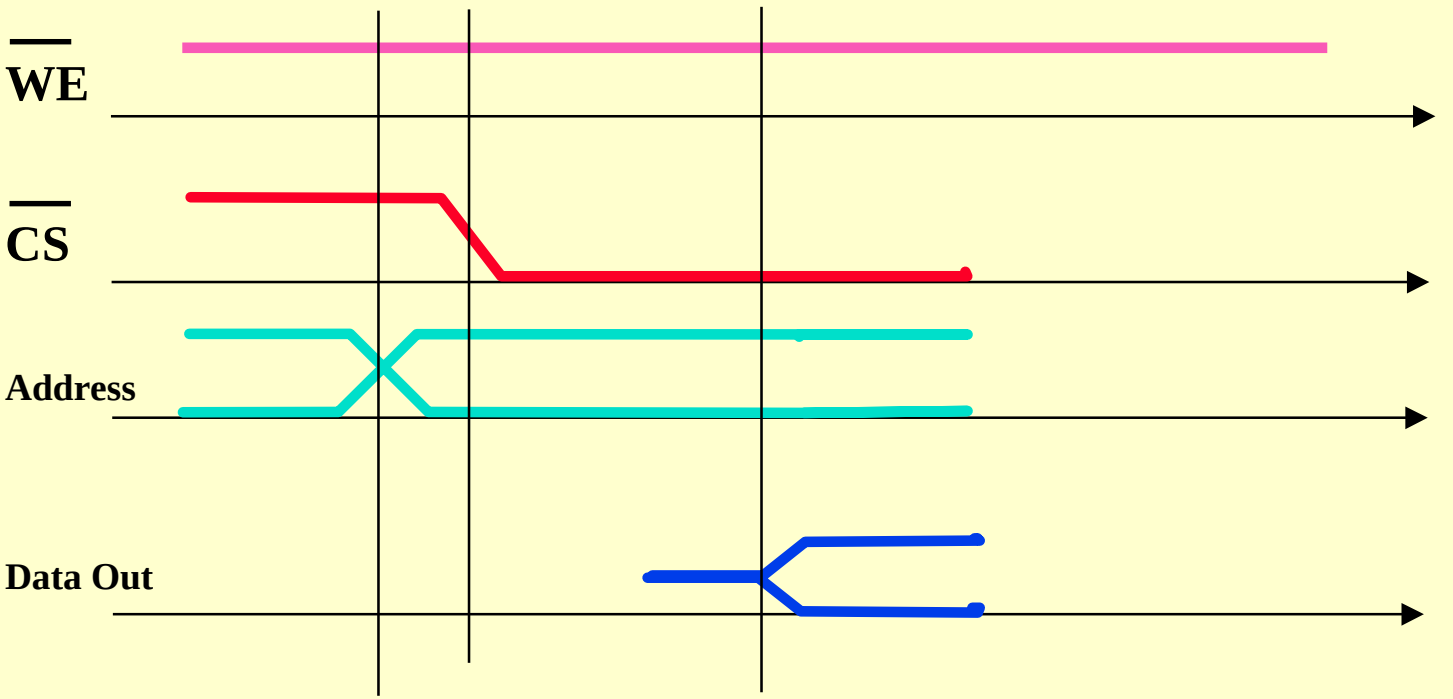
Read RAM Timing

- **READ CYCLE**



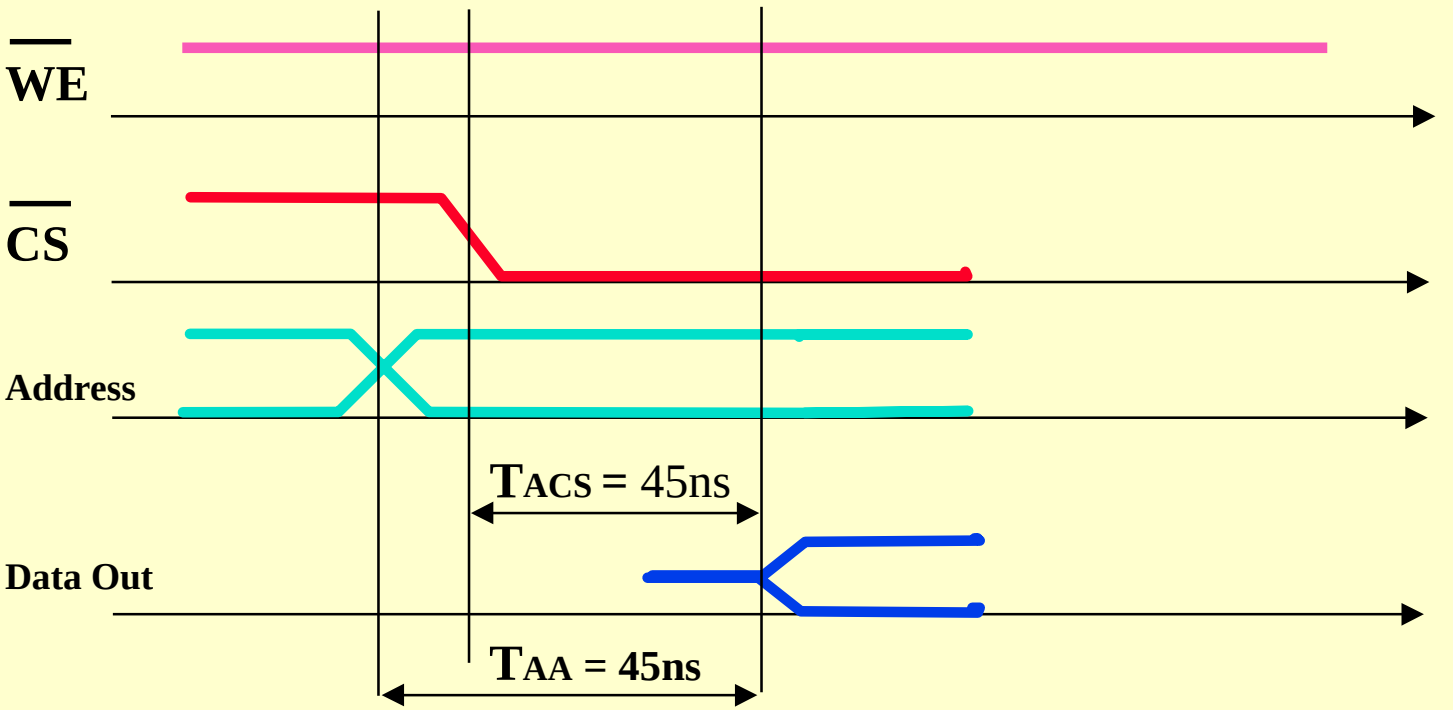
Read RAM Timing

- **READ CYCLE**



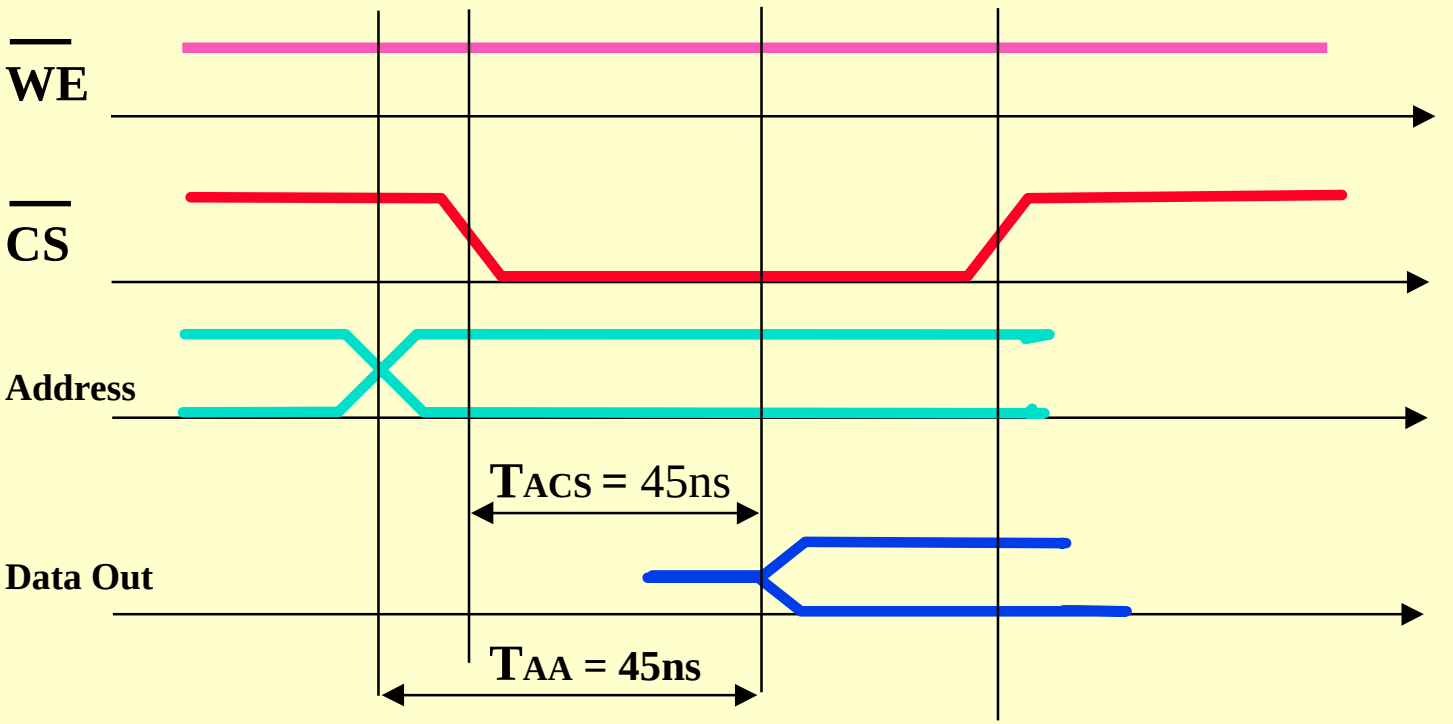
Read RAM Timing

- **READ CYCLE**



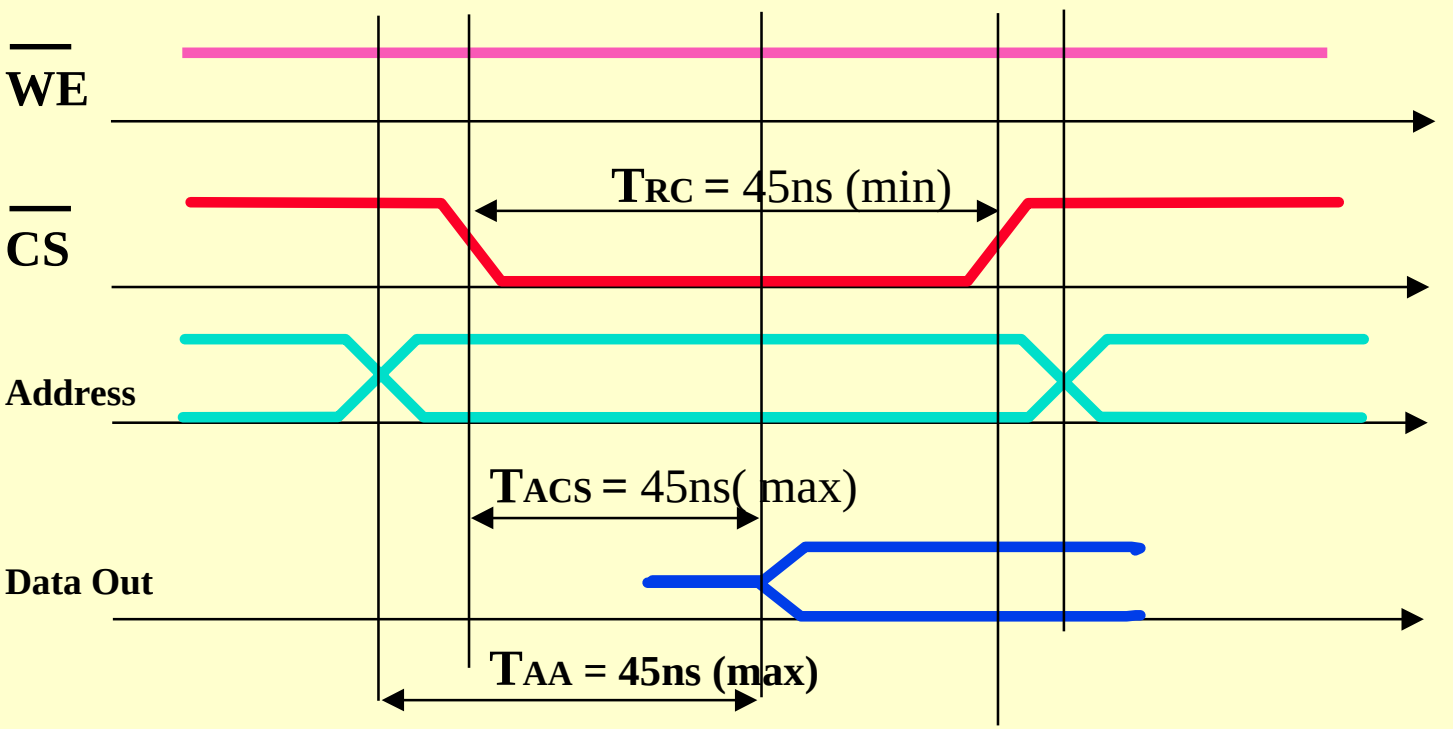
Read RAM Timing

- **READ CYCLE**



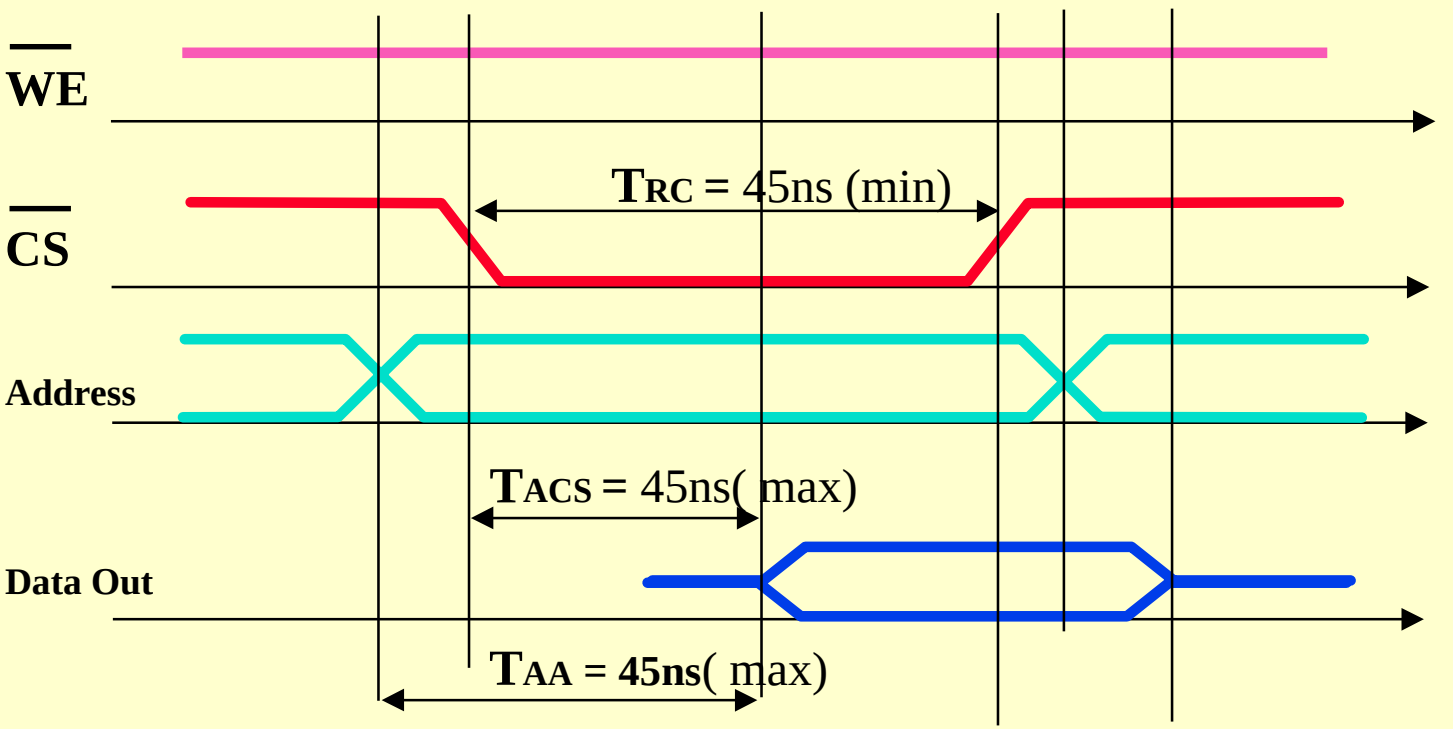
Read RAM Timing

- **READ CYCLE**



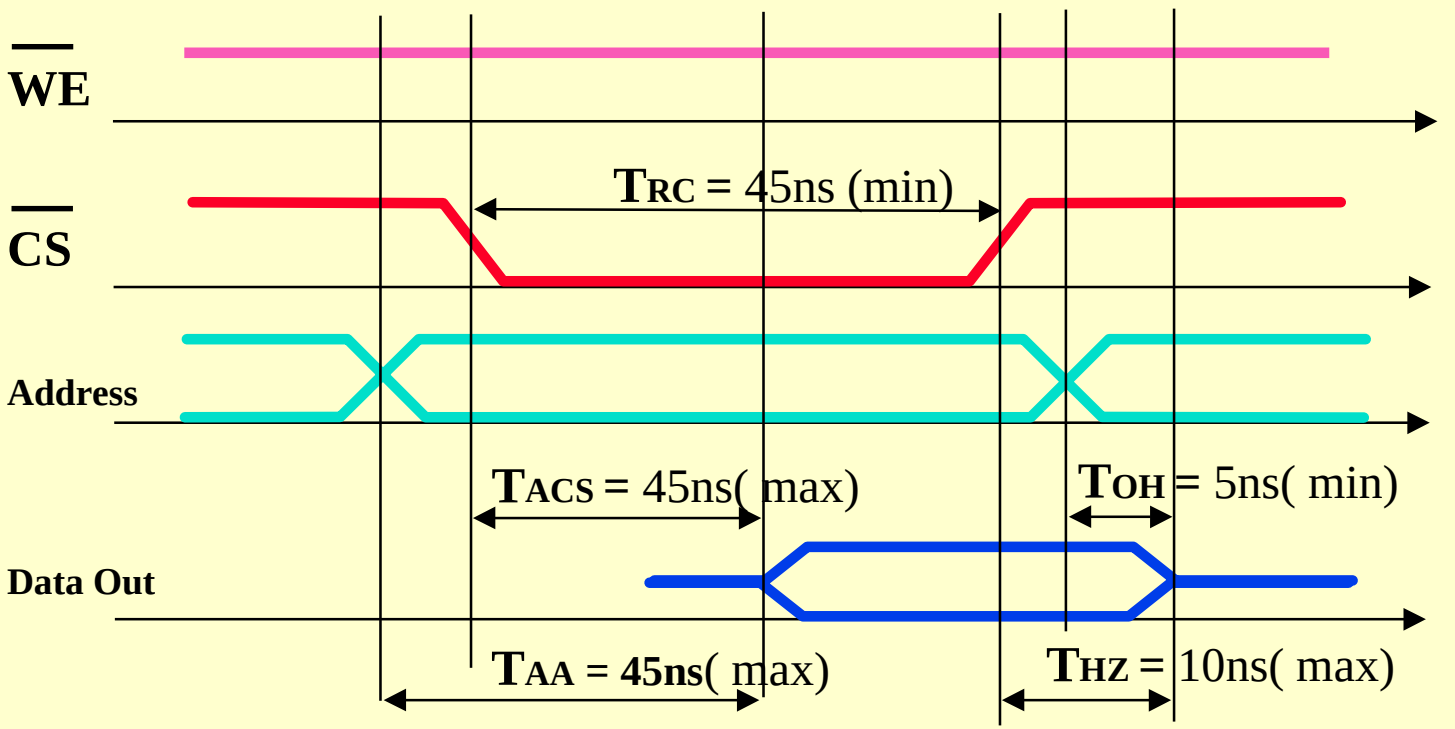
Read RAM Timing

- **READ CYCLE**



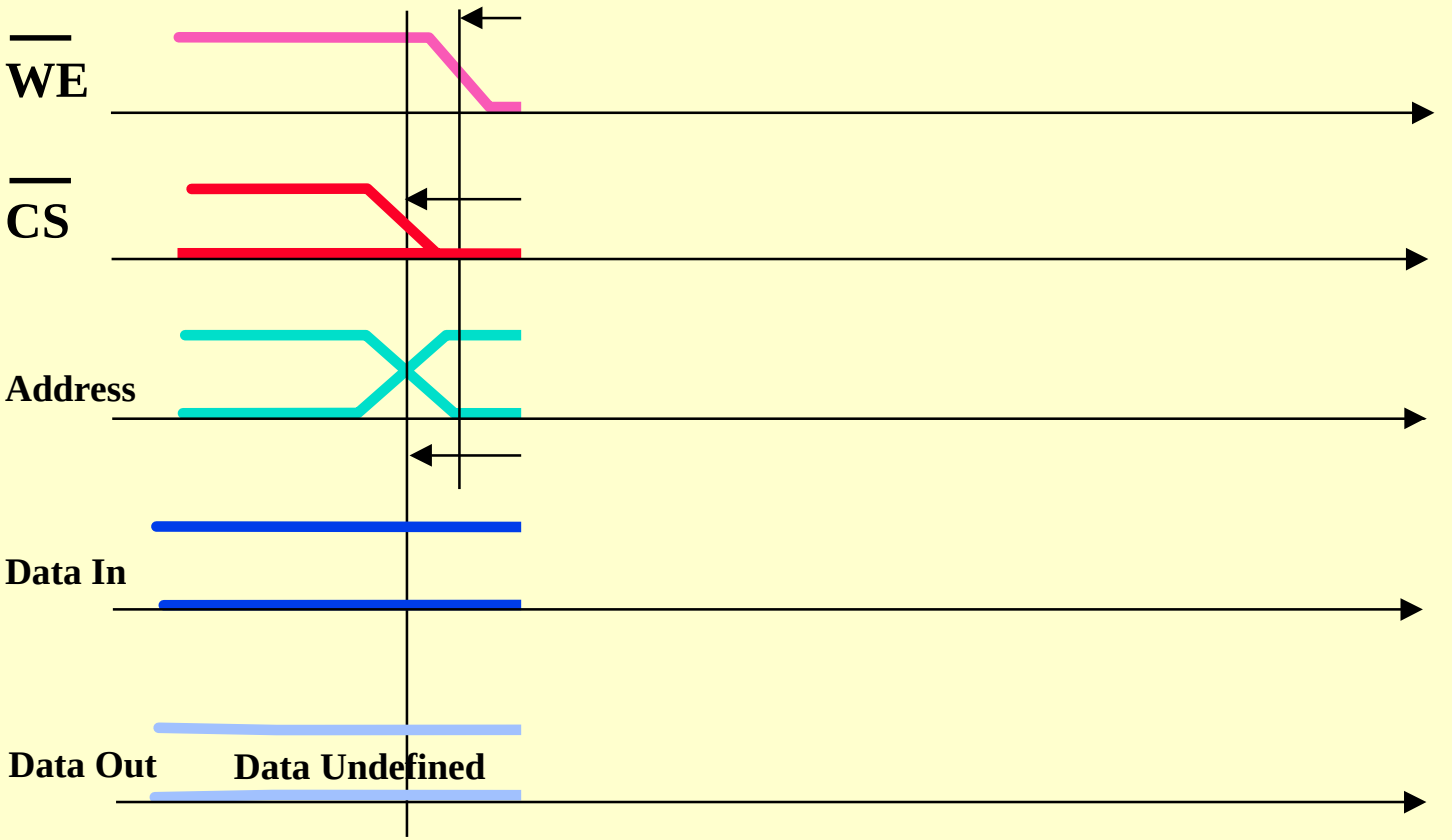
RAM Dynamic Parameters

- **READ CYCLE**



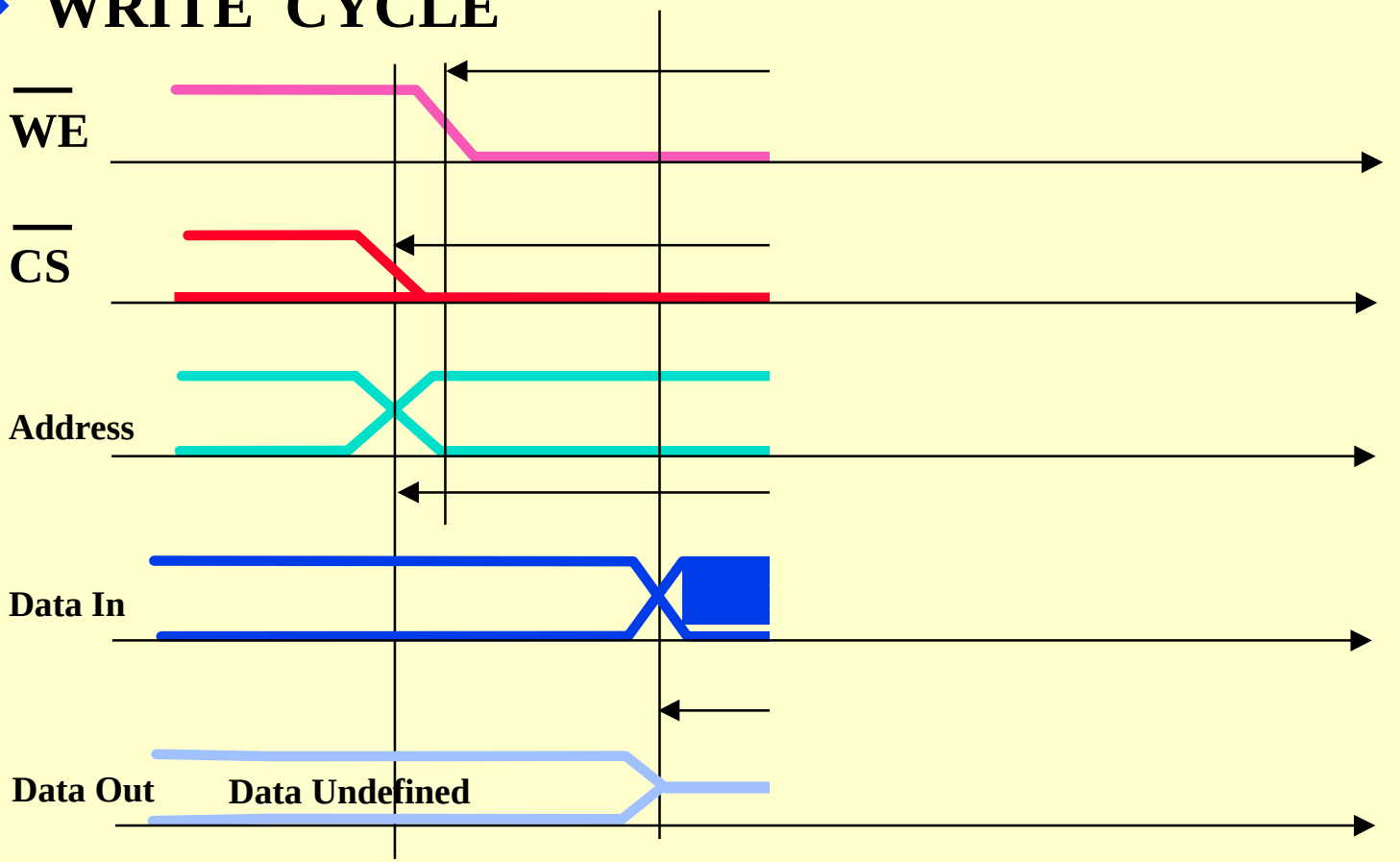
Write RAM Timing

- **WRITE CYCLE**



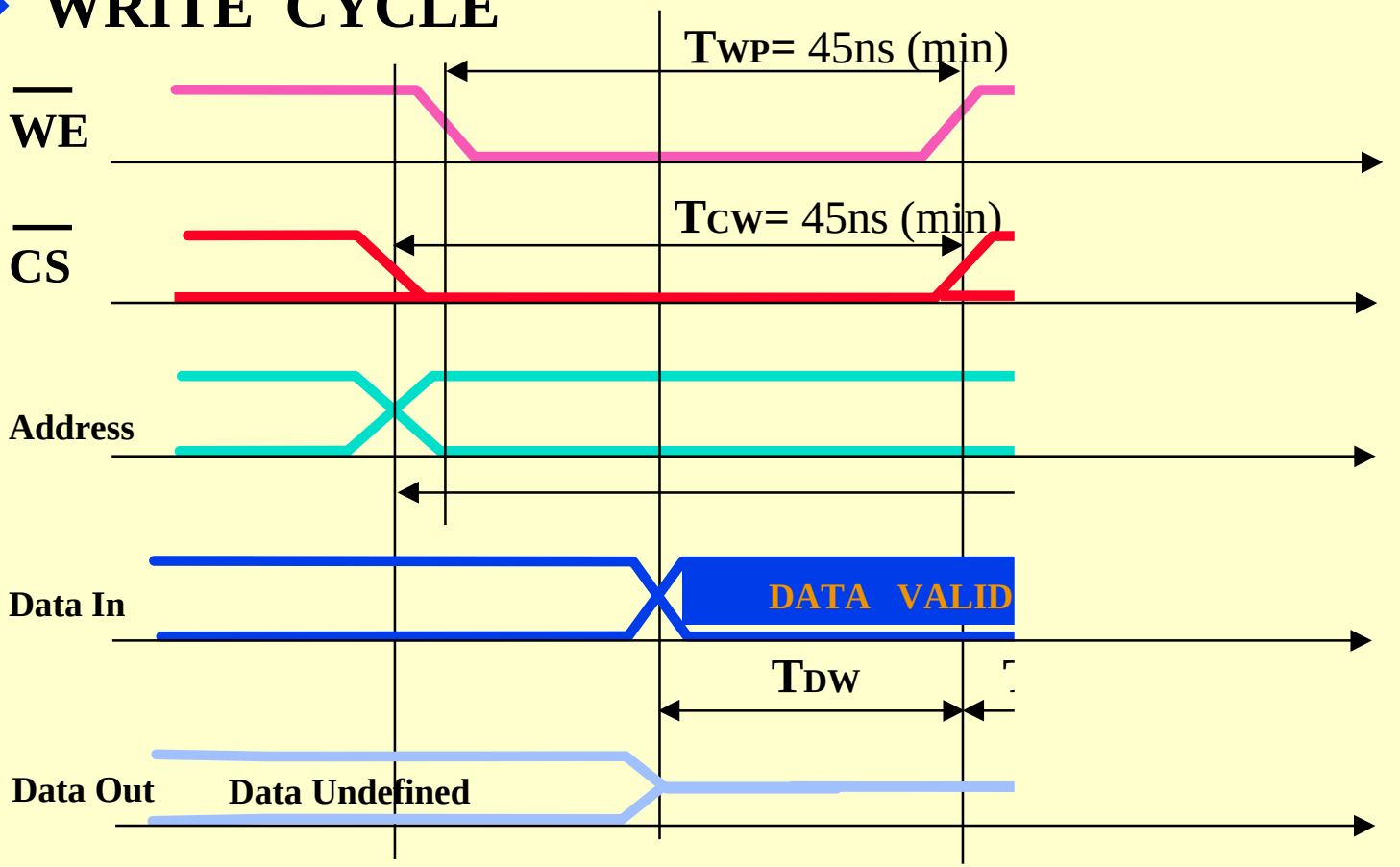
Write RAM Timing

- **WRITE CYCLE**



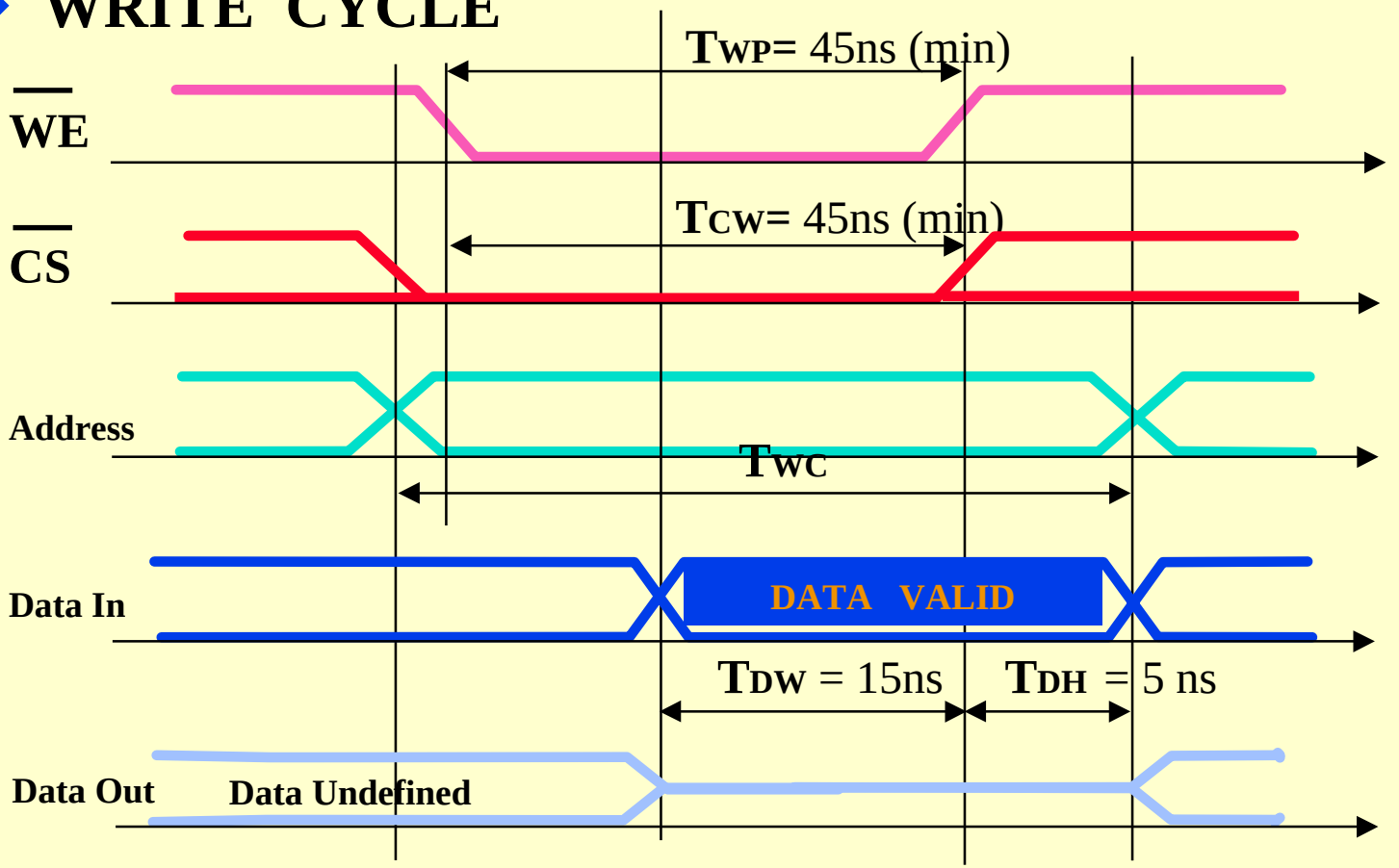
Write RAM Timing

- **WRITE CYCLE**

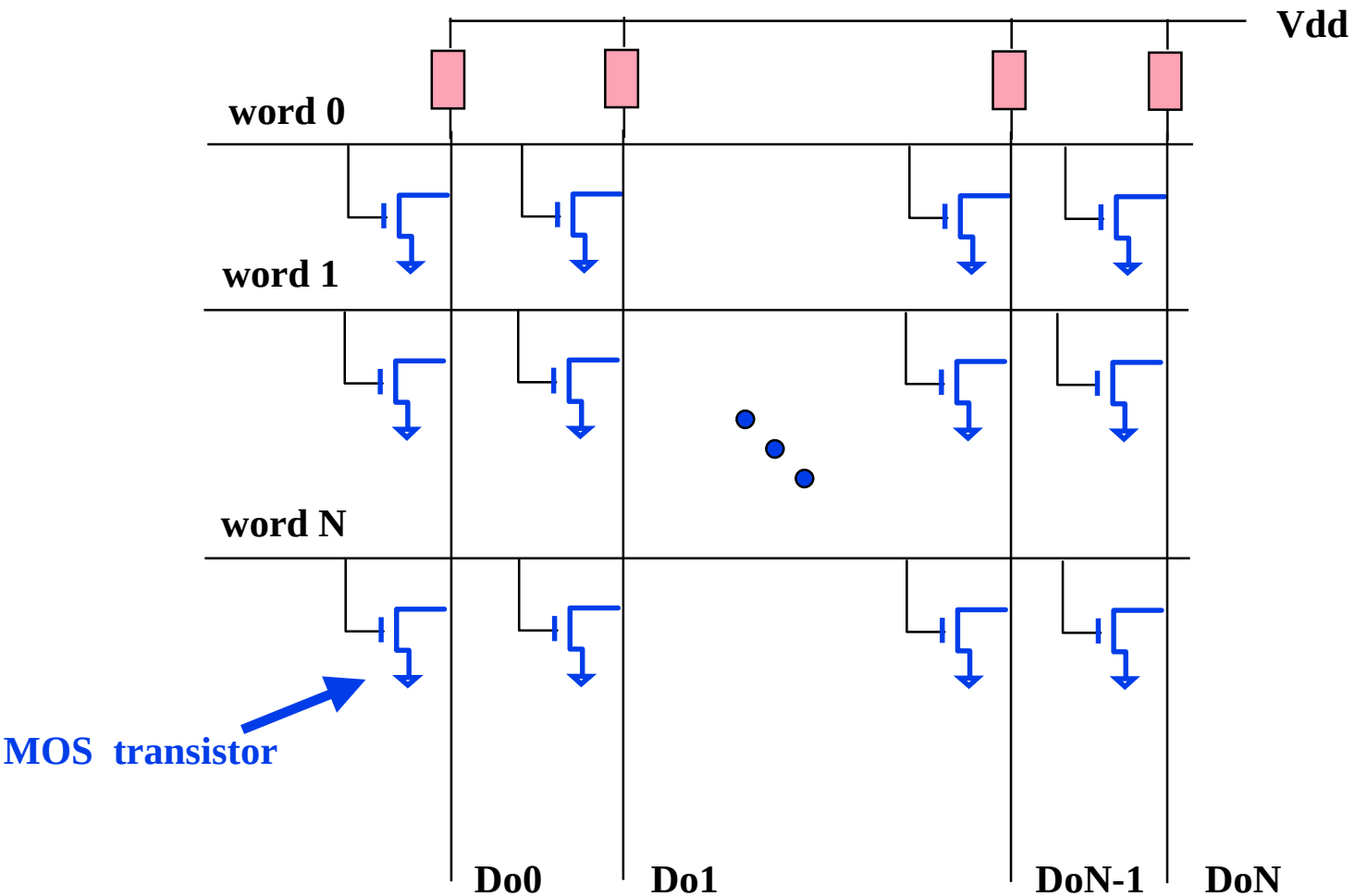


Write RAM Timing

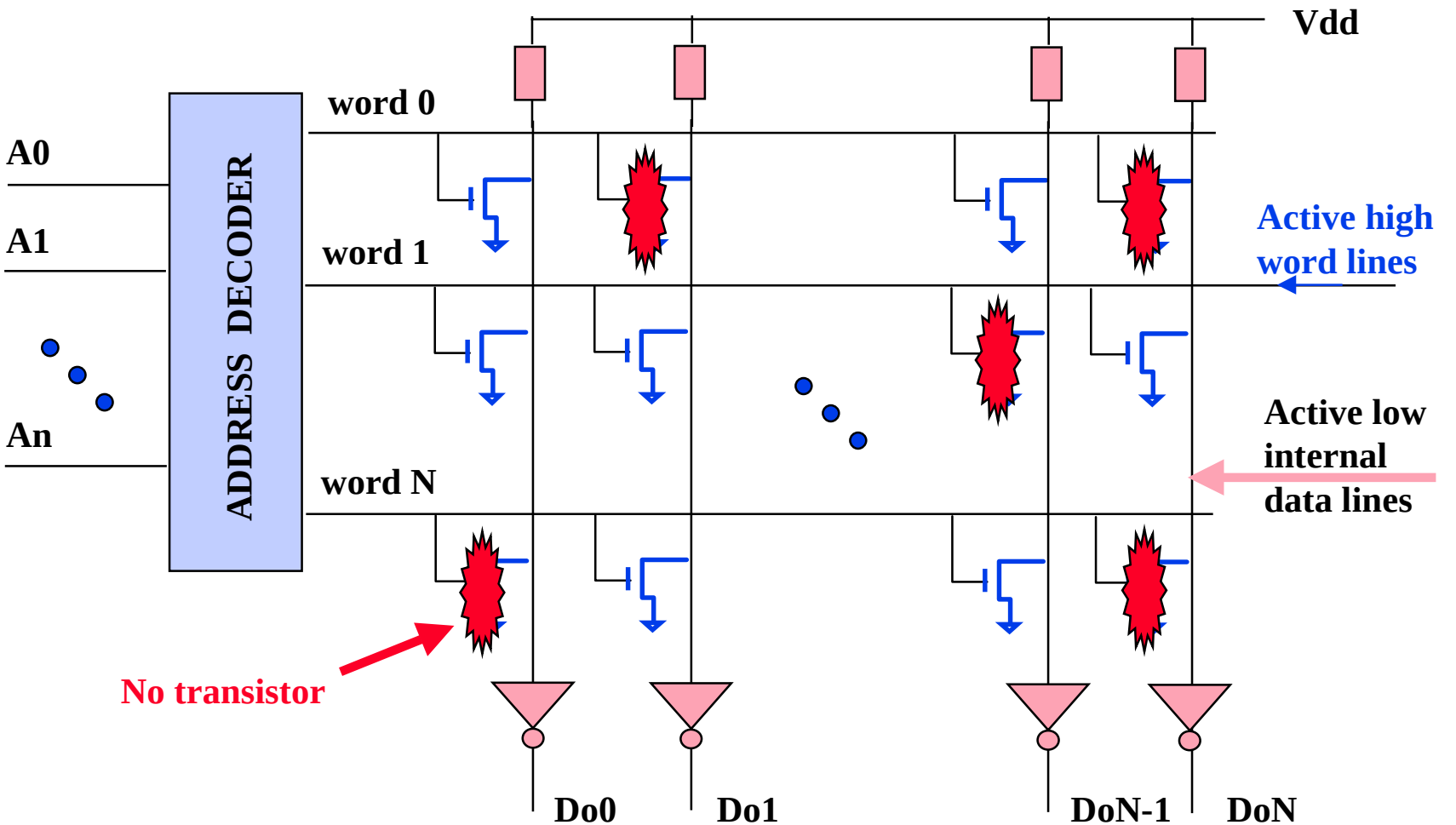
- **WRITE CYCLE**



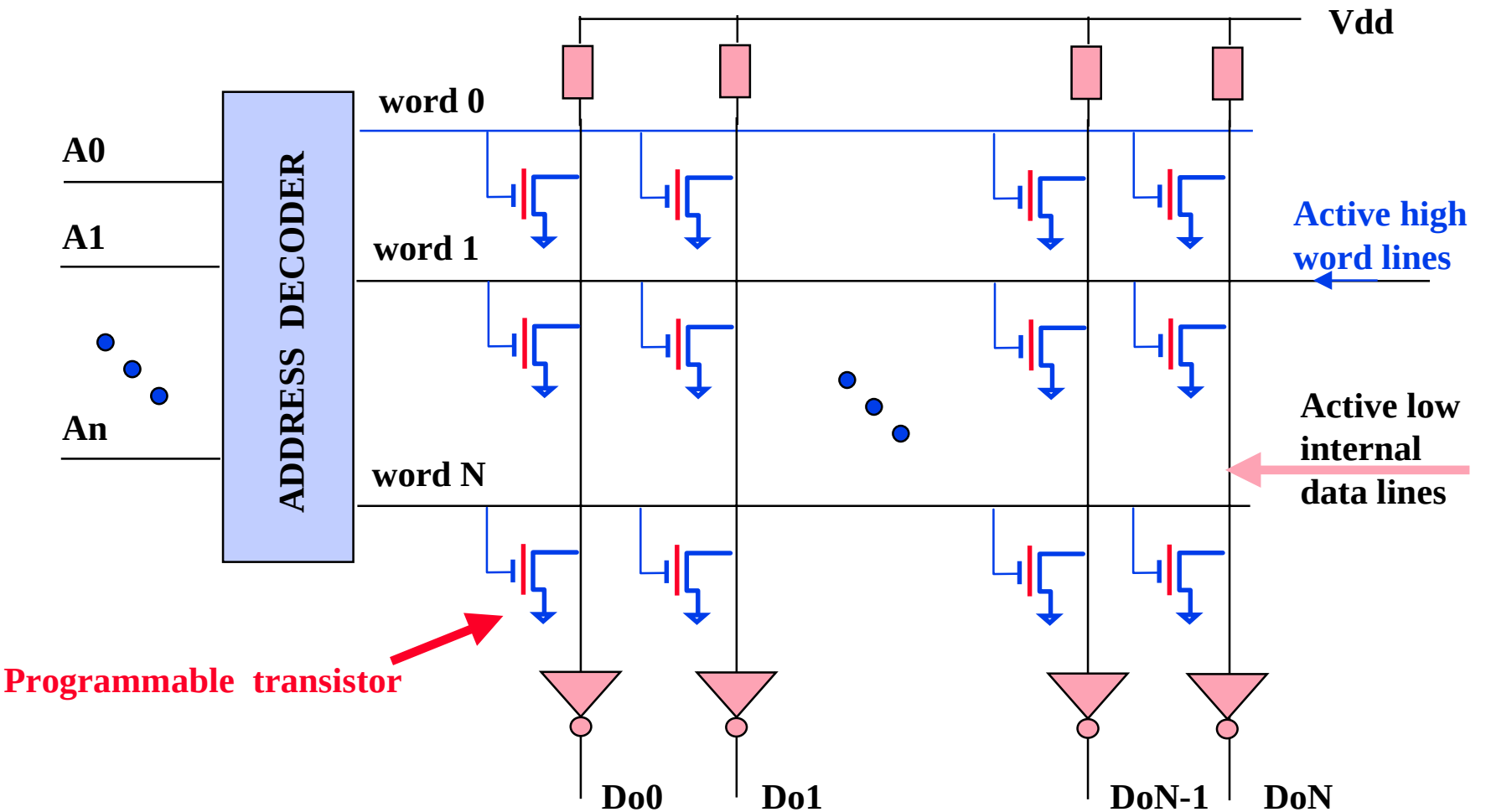
Read Only Memory - ROM



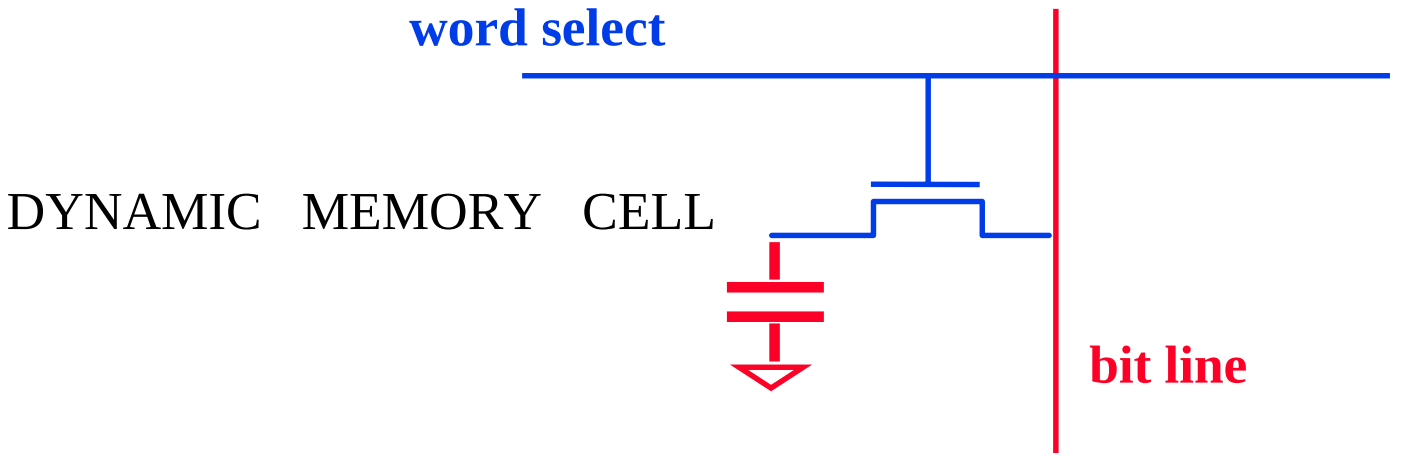
Read Only Memory - ROM



Erasable Programmable Read Only Memory - EPROM

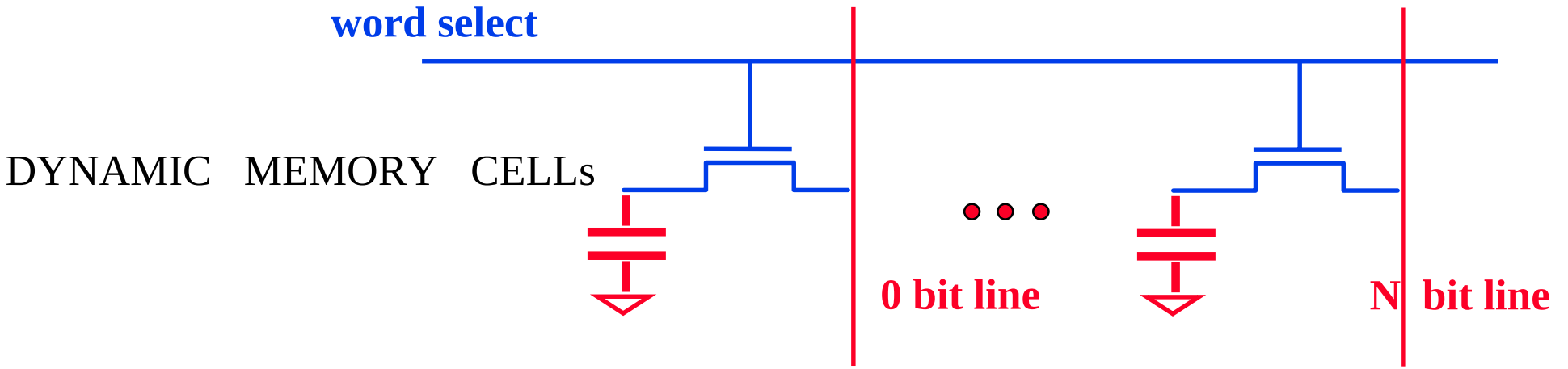


DYNAMIC RAM MEMORY

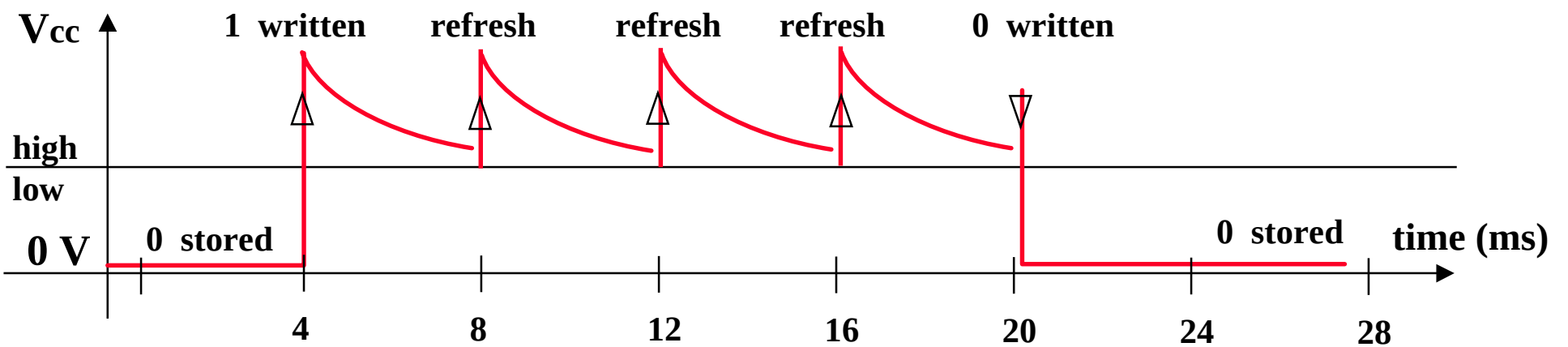


THE BASIC ELEMENT IS A CAPACITOR
THAT HOLDS THE STORED VALUE ONLY FOR A SHORT TIME.
THE STORED VALUE MUST BE 'REFRESHED" PERIODICALLY
TO PREVENT LOST OF DATA.

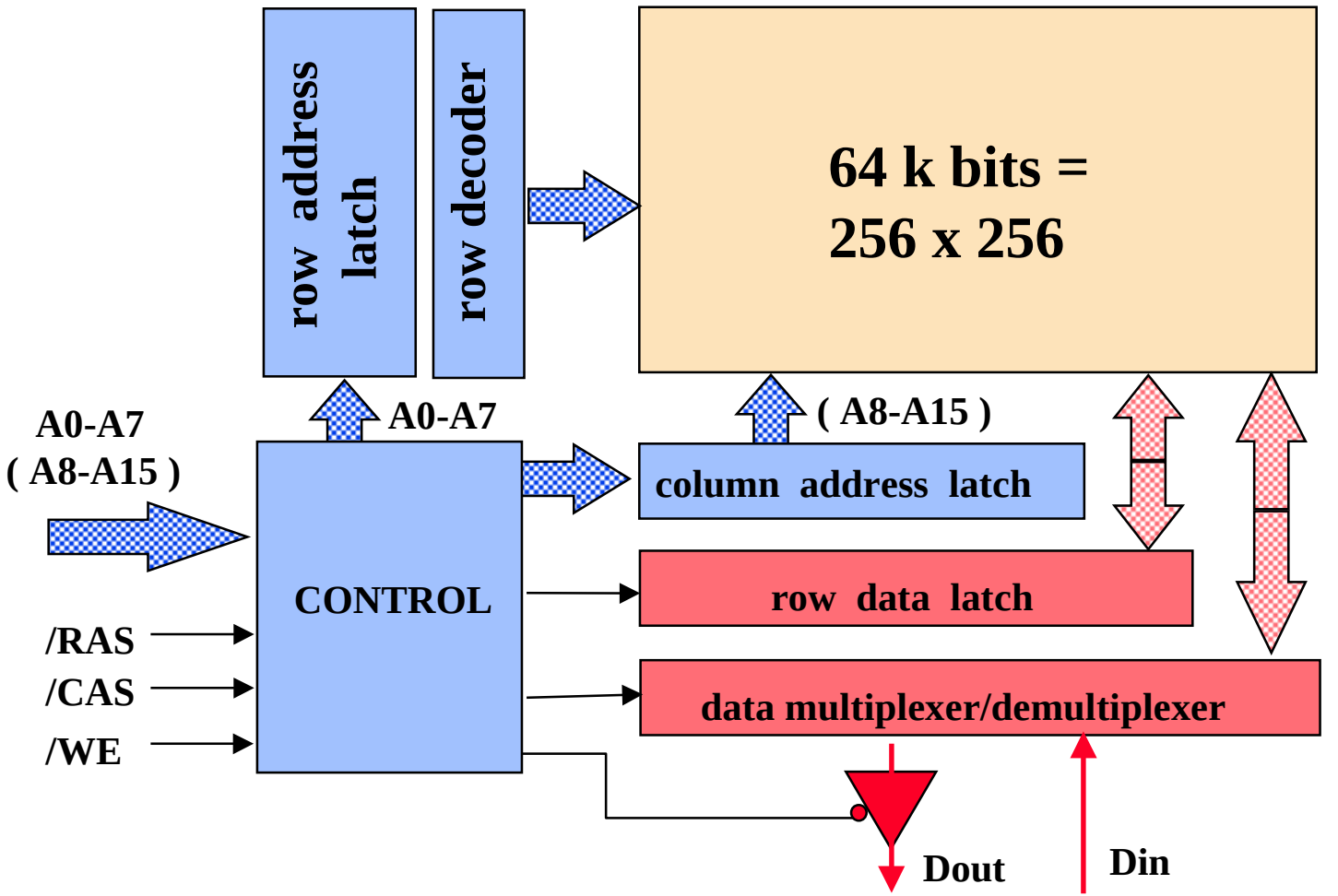
DYNAMIC RAM MEMORY



STORE AND REFRESH OPERATION

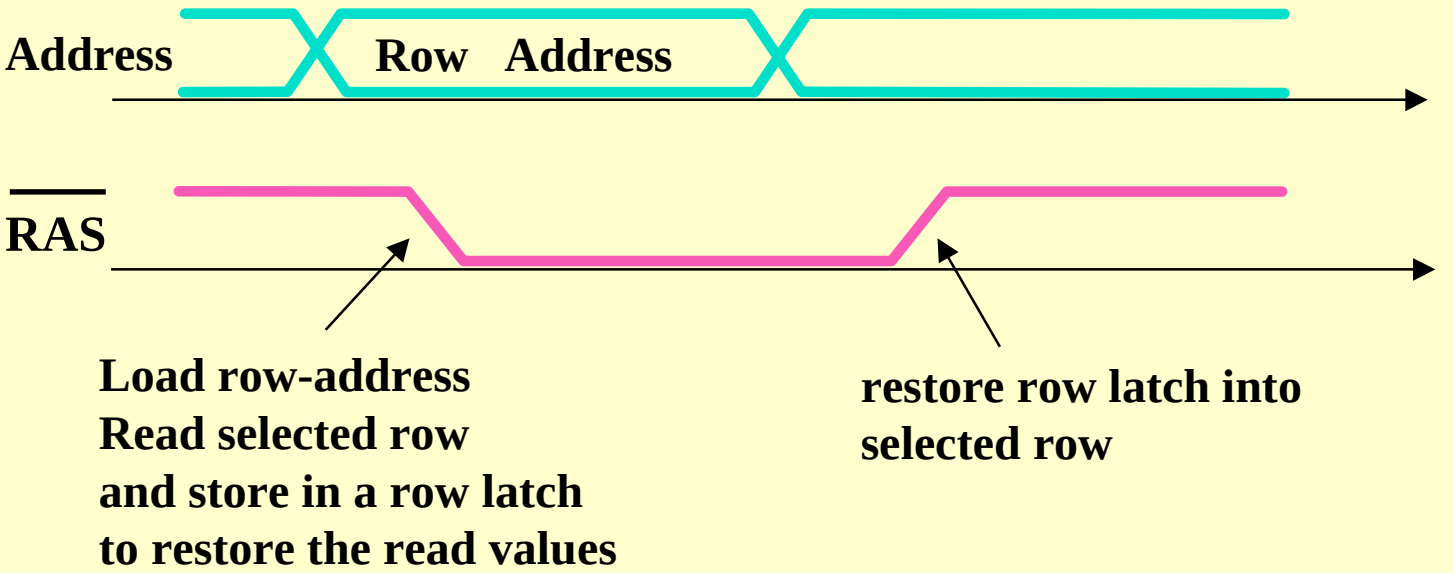


DYNAMIC RAM MEMORY



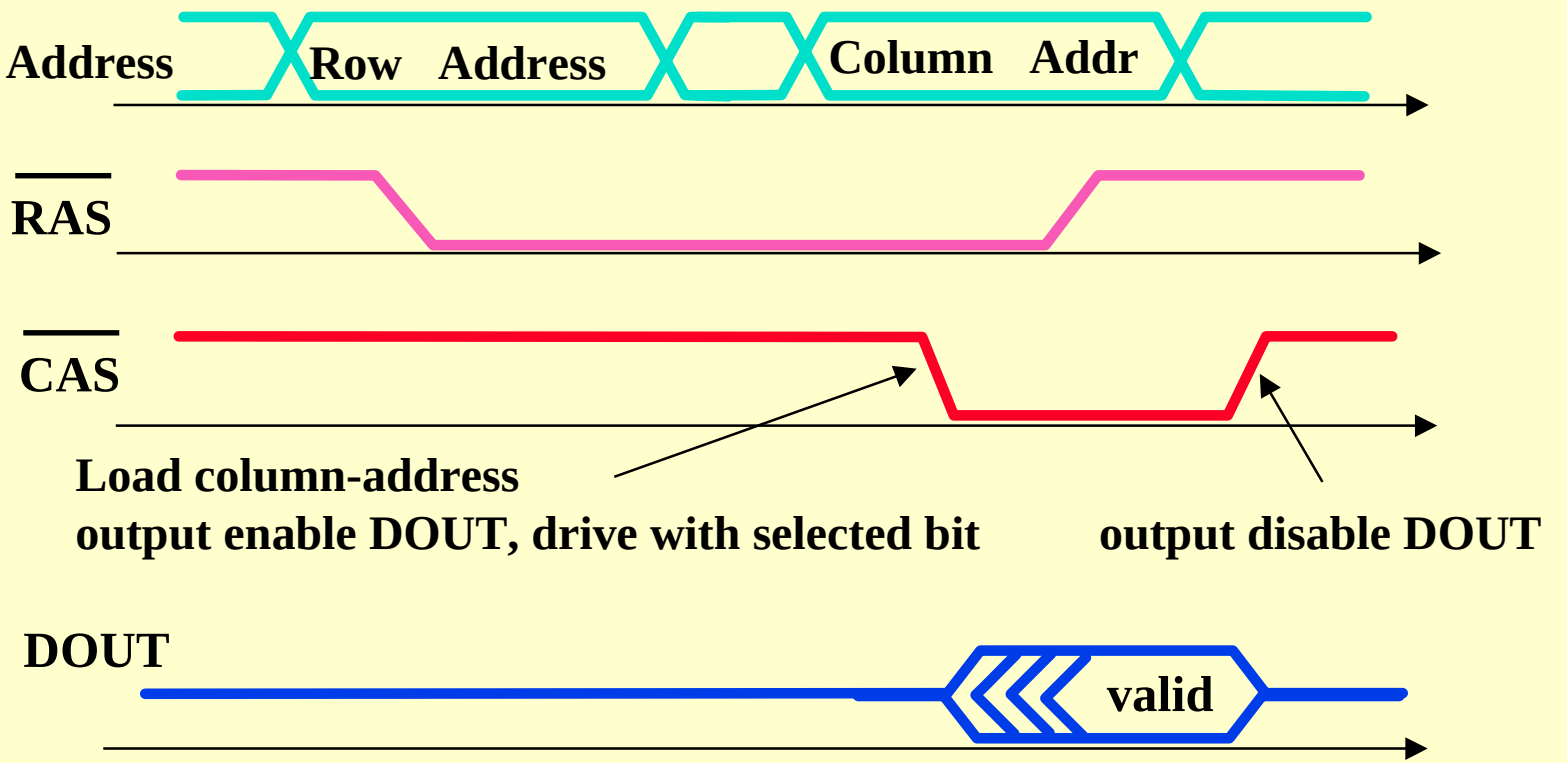
Dynamic RAM Timing

- **RAS ONLY REFRESH CYCLE**



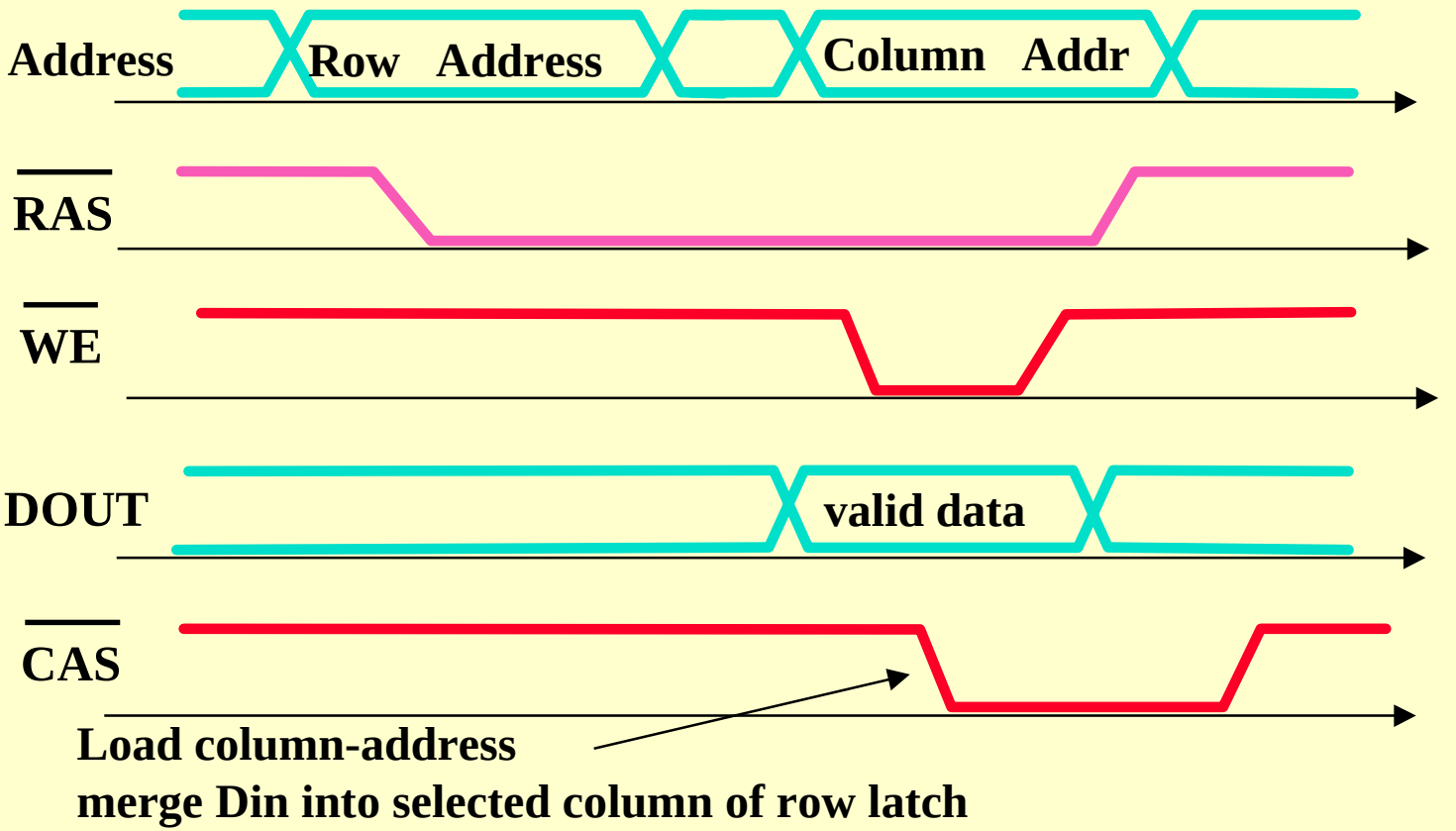
Dynamic RAM Timing

- **READ CYCLE**



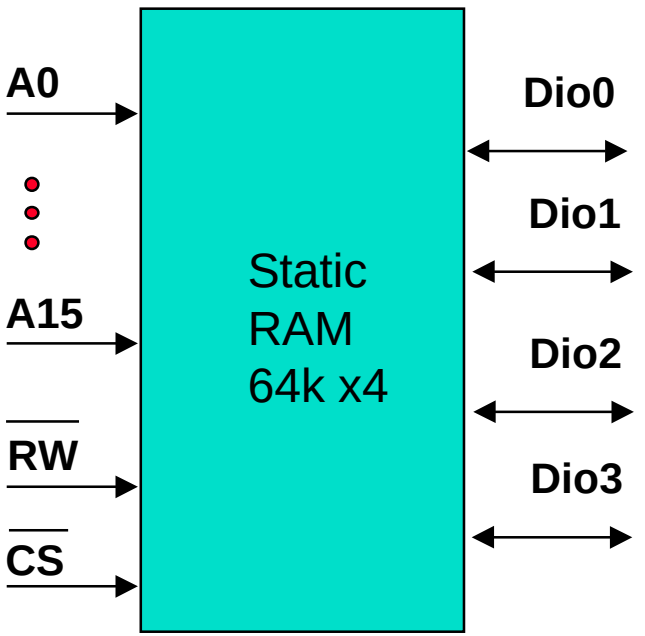
Dynamic RAM Timing

- **WRITE CYCLE**



MEMORY SYSTEM

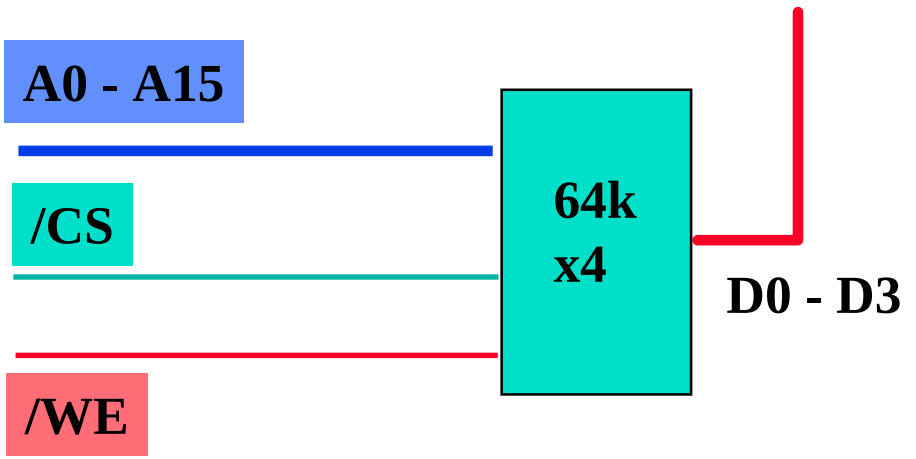
- Build a 128k x 8 static RAM memory system of RAM chips 64k x 4bit.



A0 - A15 - address lines
Dio0 - Dio3 - input/output
tri-state data lines
RW - read/write active low
CS - chip select active low

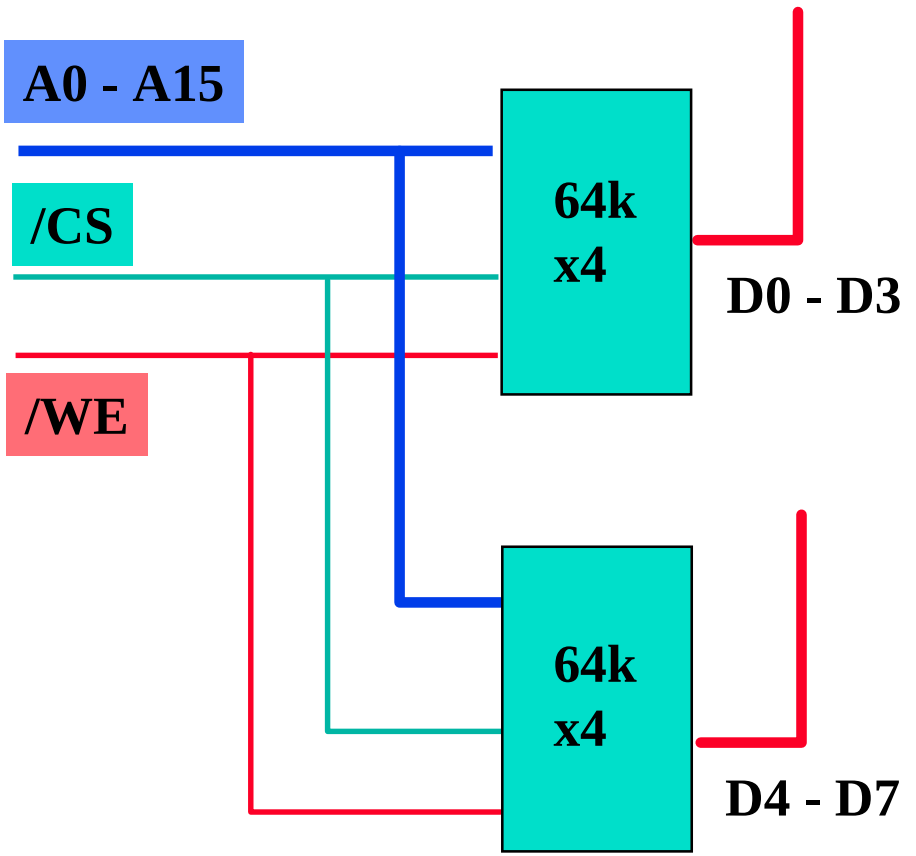
CS	RW	Function
0	0	Read
0	1	Write
1	x	Dio0-Dio3 in TriState

MEMORY SYSTEM 128k x8



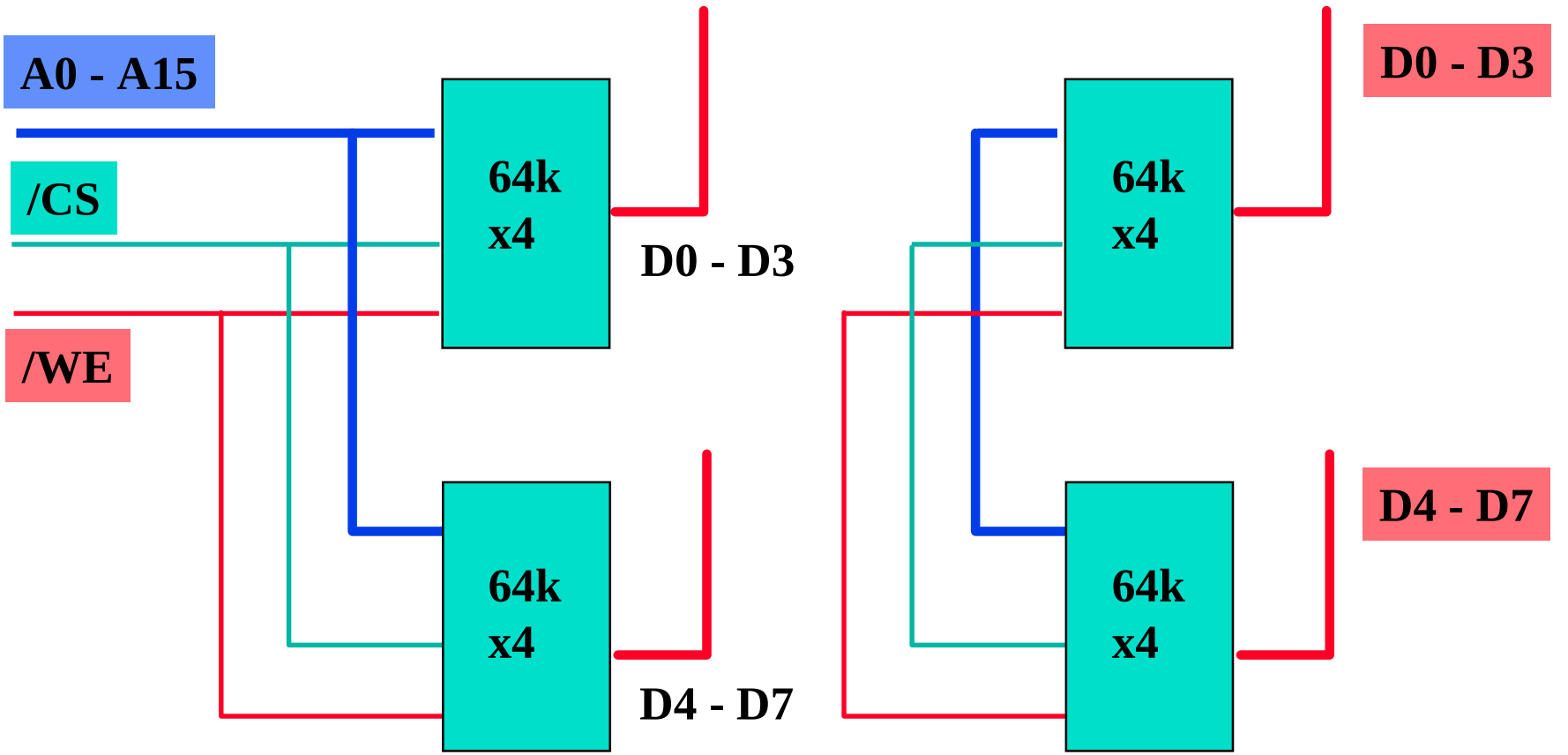
MEMORY SYSTEM 64K x 4

MEMORY SYSTEM 128k x8

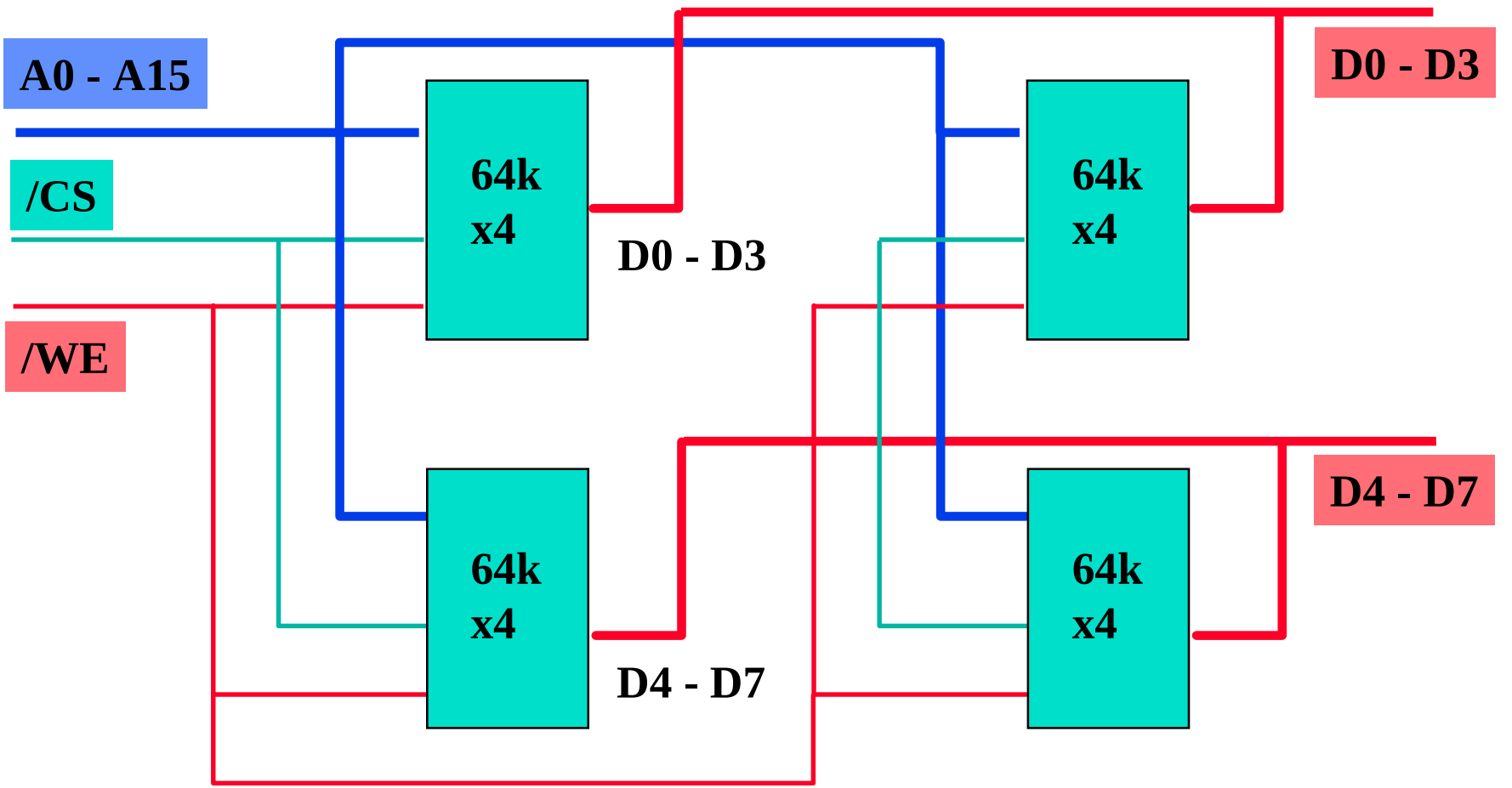


MEMORY SYSTEM 64K x 8

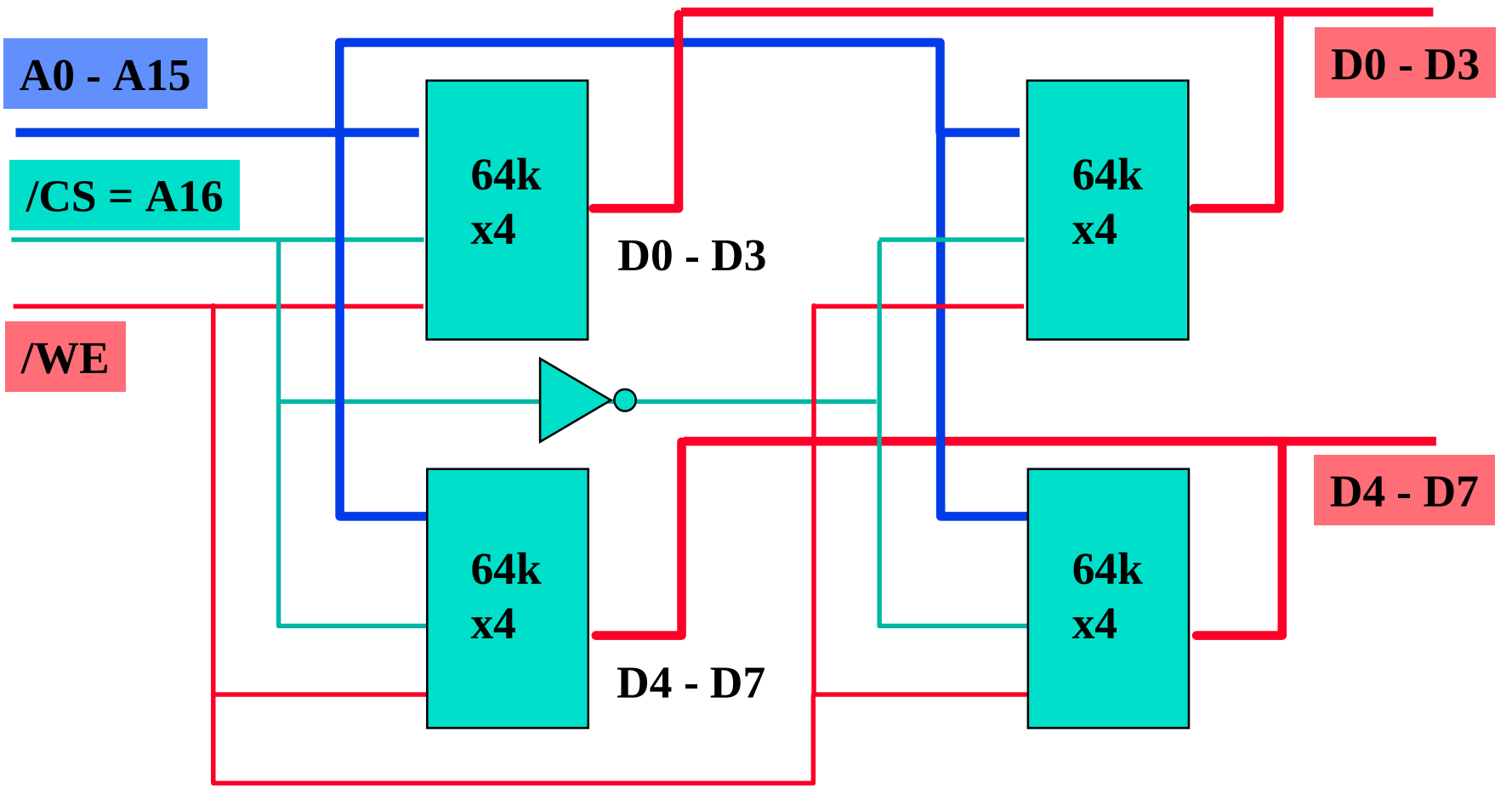
MEMORY SYSTEM 128k x8



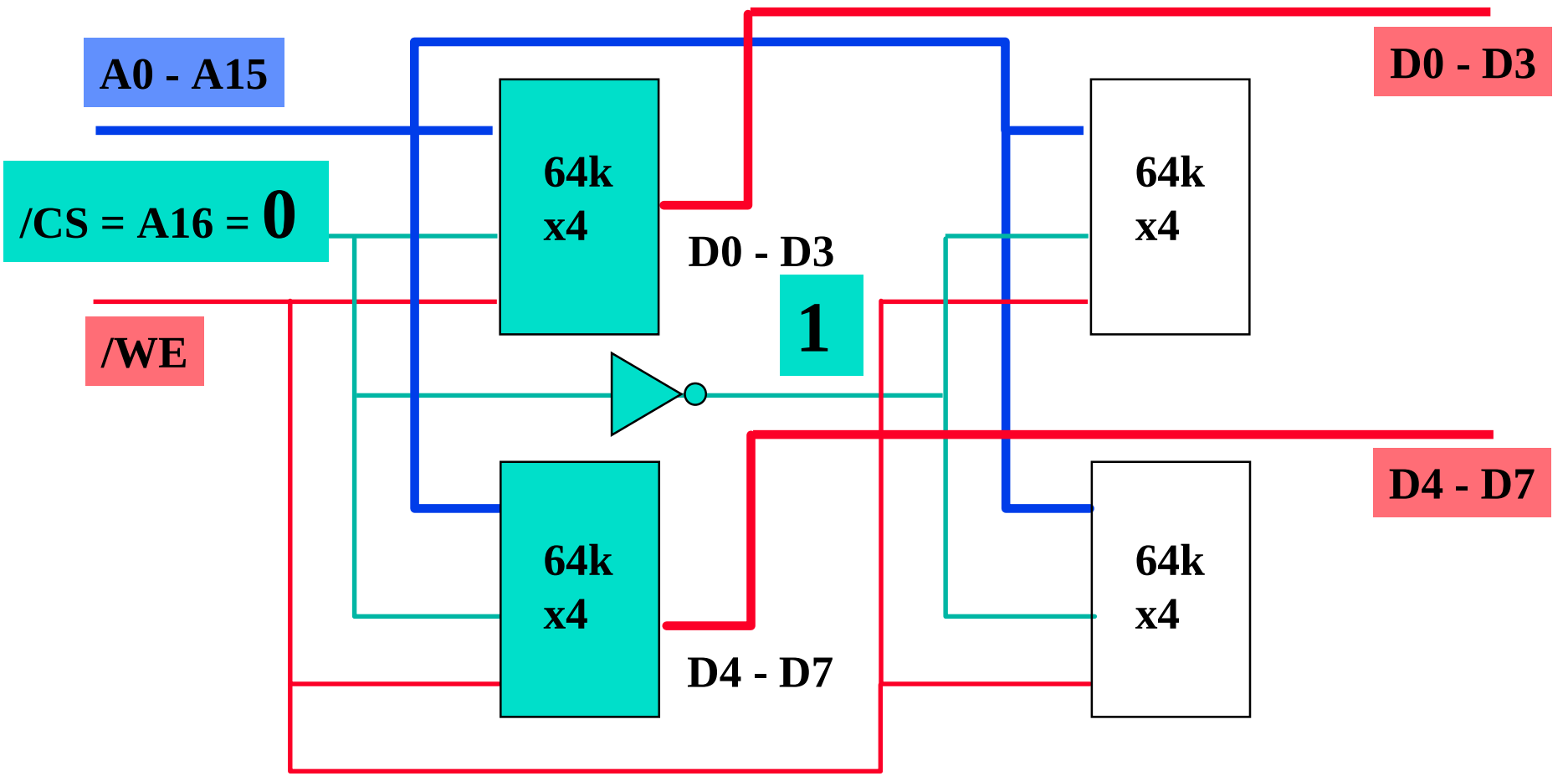
MEMORY SYSTEM 128k x8



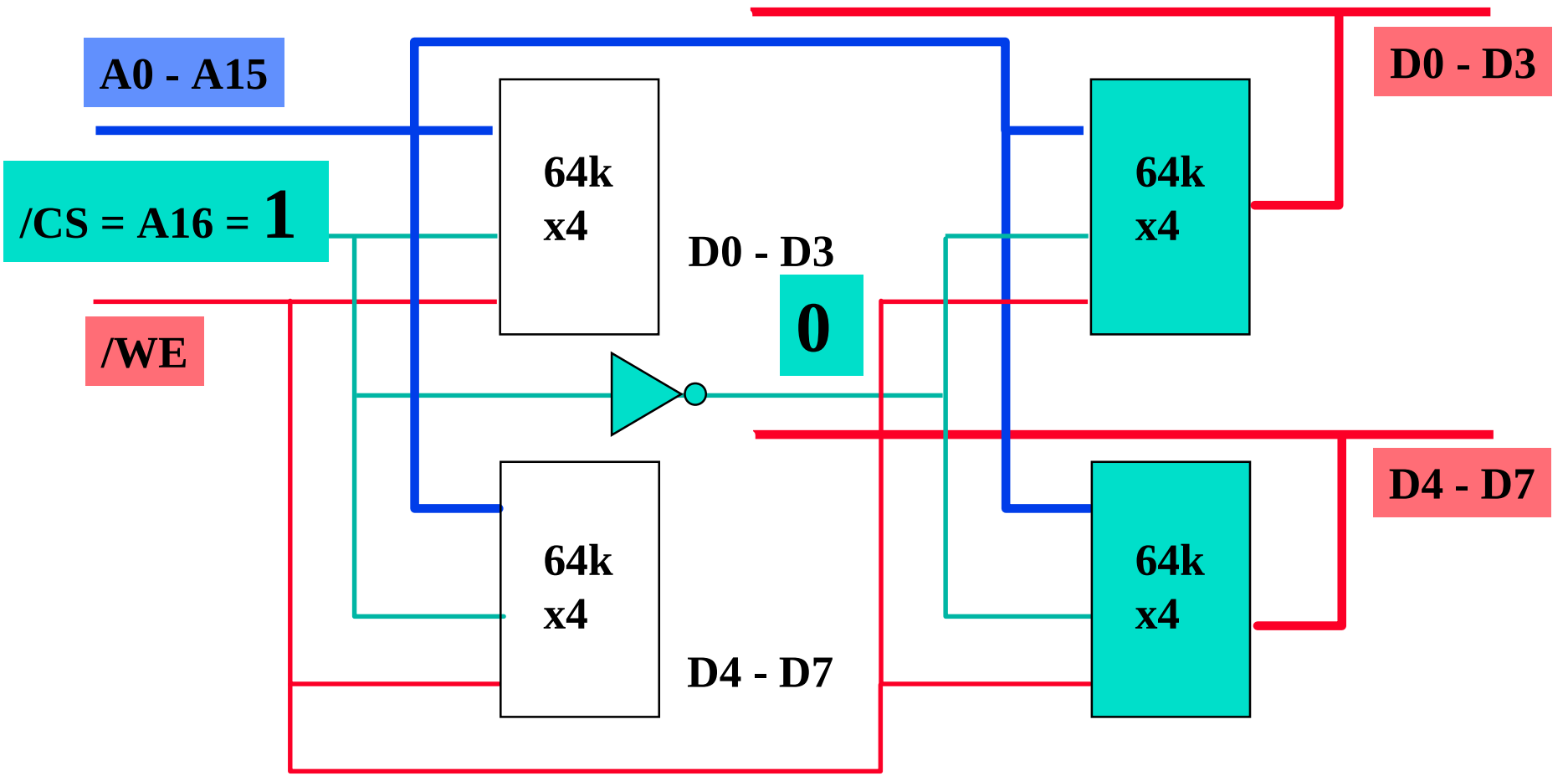
MEMORY SYSTEM 128k x8



MEMORY SYSTEM 128k x8



MEMORY SYSTEM 128k x8



What have we learnt?

- RAM - Random Access Memory allow to read/write data at a randomly chosen address to the contrary of a floppy disk where the data is stored and accessed in sequence.
- ROM - Read Only Memory allows to read data stored (during programming) at a randomly chosen address.
- EPROM allows to program the contents of the memory and later read it.Programming is much slower than reading.
- Dynamic RAM achieve the largest density and is the prevalent technology for computer memories.
- Memory chips can be organised in memory systems of various depth and width.